

MODEL NAME : *AAM00*

PCB NO : *LA-C361P*

BOM P/N :

Dell/Compal Confidential

Schematic Document

SKYLAKE-H

2014-05-22

Rev: 0.0 (M00)

@ : Nopop Component

CONN@ : Connector Component

R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB

TPM@ : TPM function

EMC@ : Pop of EMI parts

VRAMS@ : Samsung GDDR5 for GPU

VRAMH@ : Hynix GDDR5 for GPU

VRAMM@ : Micron GDDR5 for GPU

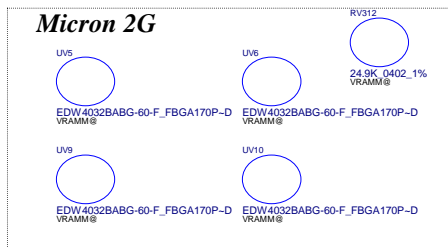
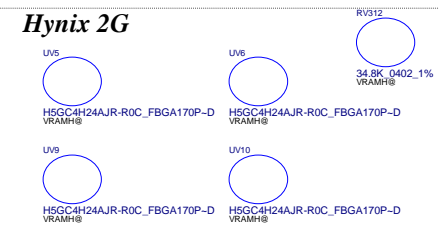
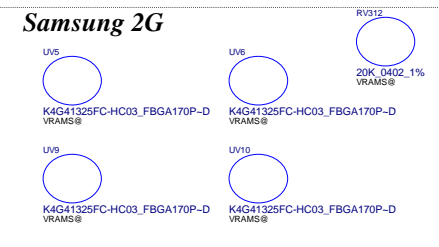
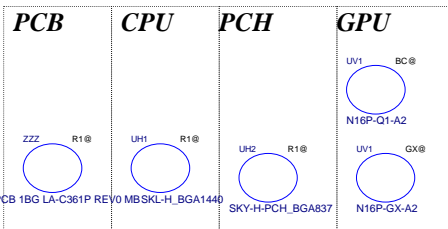
BreakDown@ : for measure power consumption

CSMB@ : CSMB sku

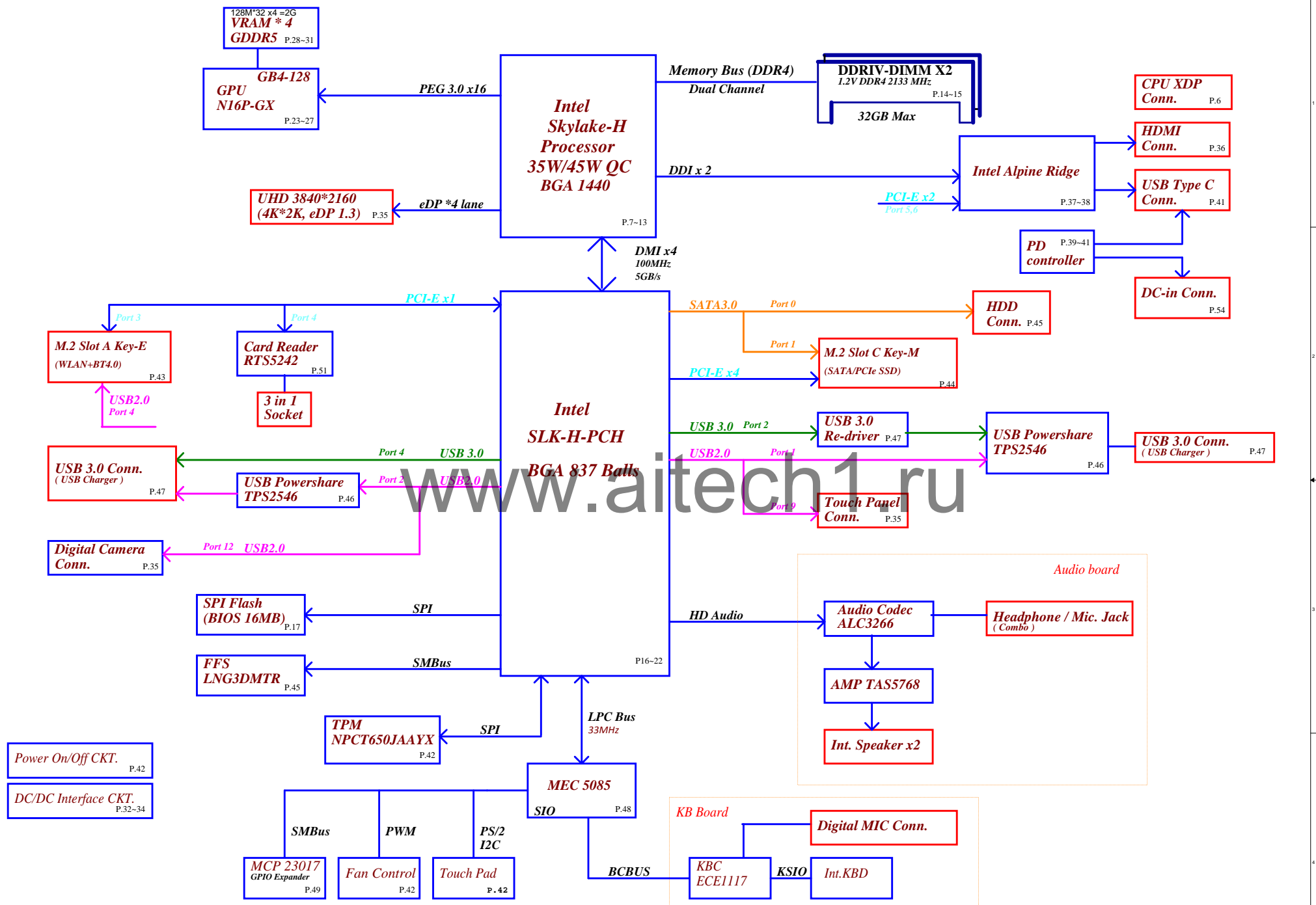
BC@ : BC sku (GPU N16P-Q1)

GX@ : GPU N16P-GX

UMA@ / DIS@ : UMA/DIS



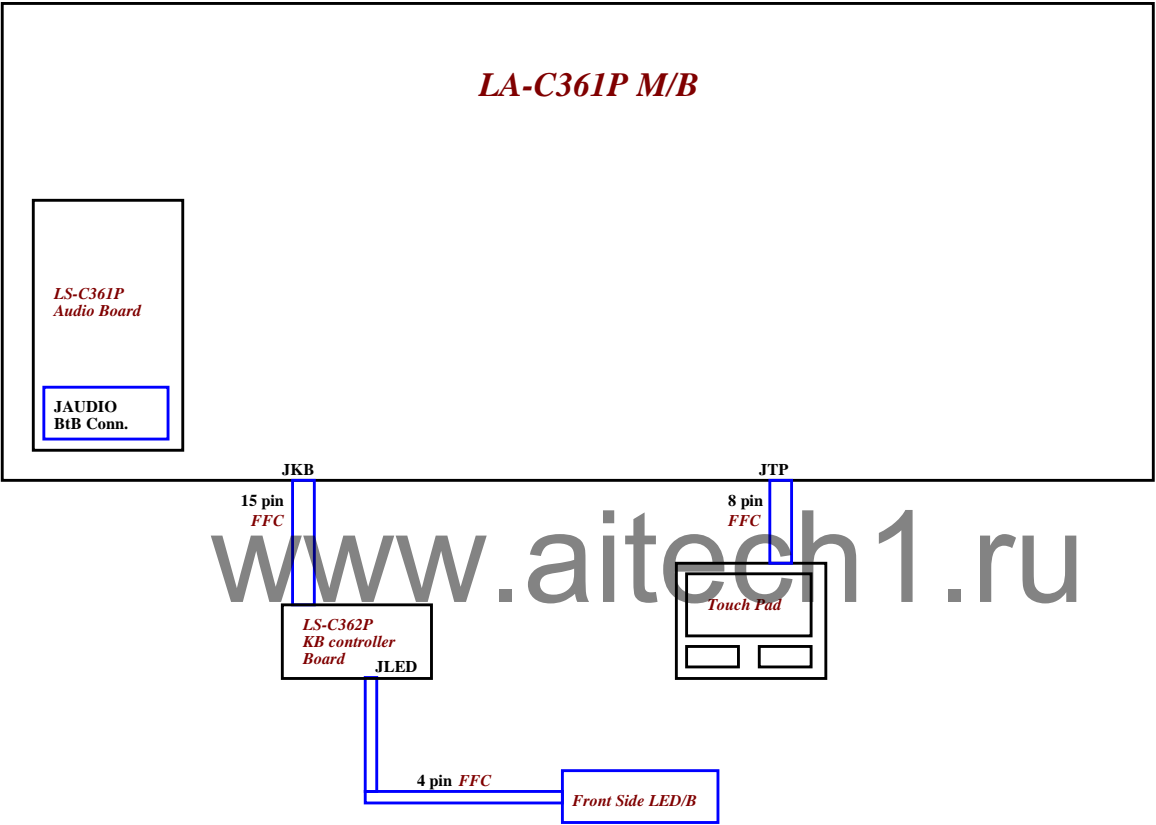
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Document Number				Rev	
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Project Code : AAM00

File Name :



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Board ID	Resistor
X00	N/A
X01	
X02	
X03	
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA



DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

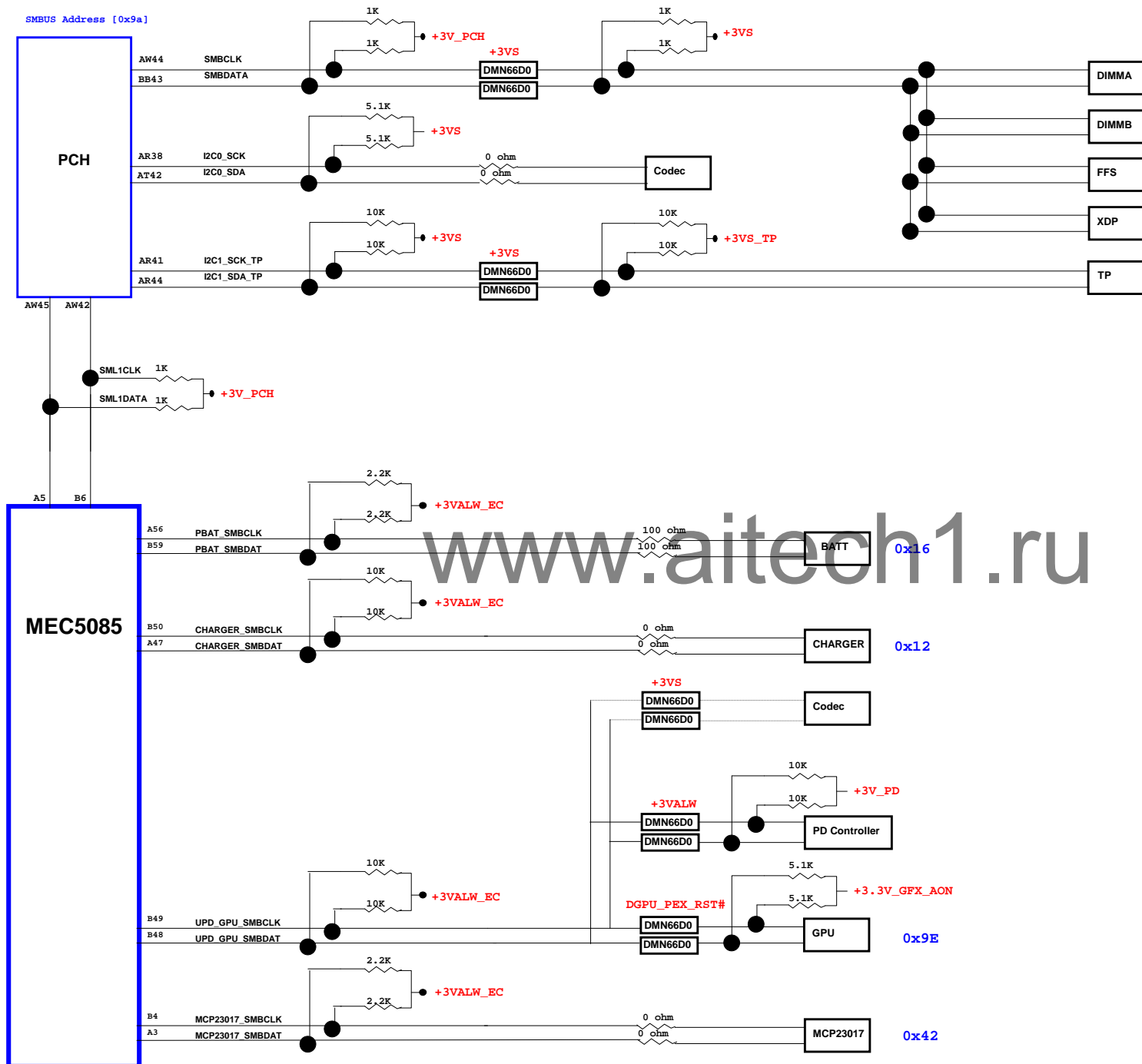
LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

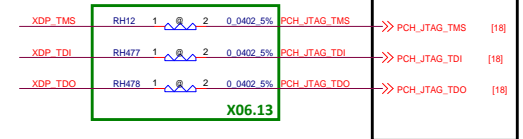
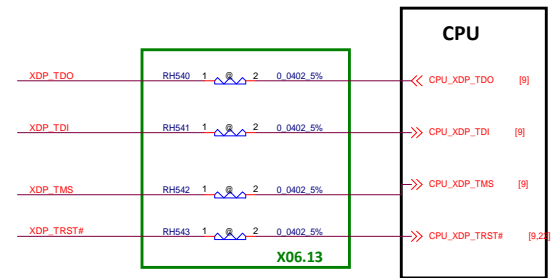
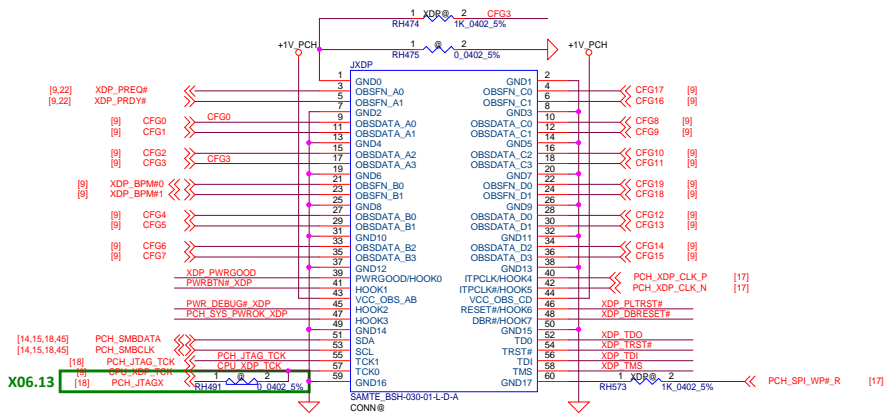
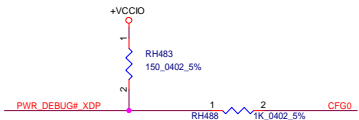
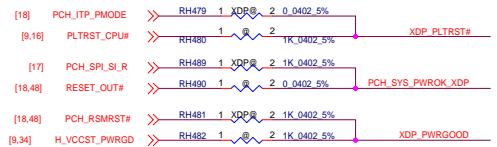
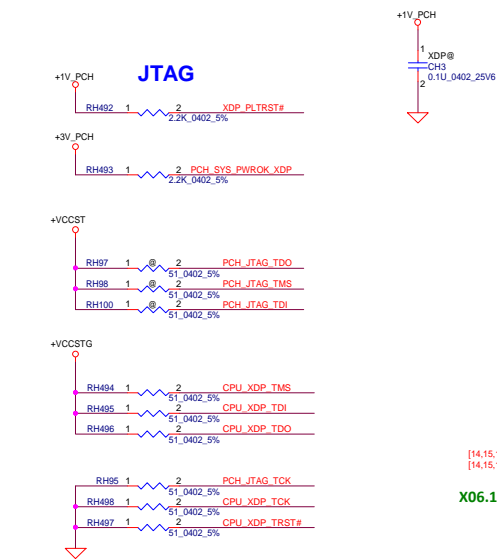
PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	CARD READER	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None	SATA	DESTINATION
Lane 9	SSD	0A	SSD
Lane 10	SSD	1A	N/A
Lane 11	SSD	N/A	N/A
Lane 12	SSD	N/A	N/A
Lane 13	None	0B	None
Lane 14	None	1B	HDD
Lane 15	Alpine Ridge	2	None
Lane 16		3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

Symbol Note :

 : means Digital Ground
  : means Analog Ground



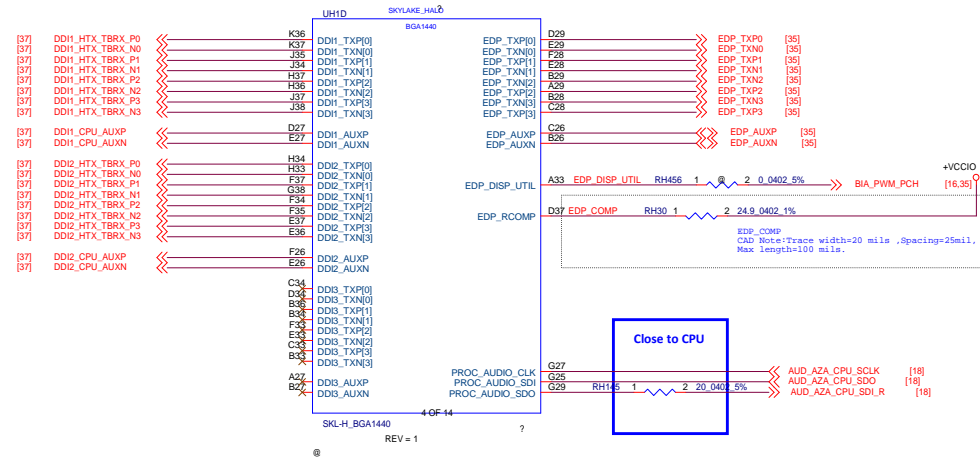


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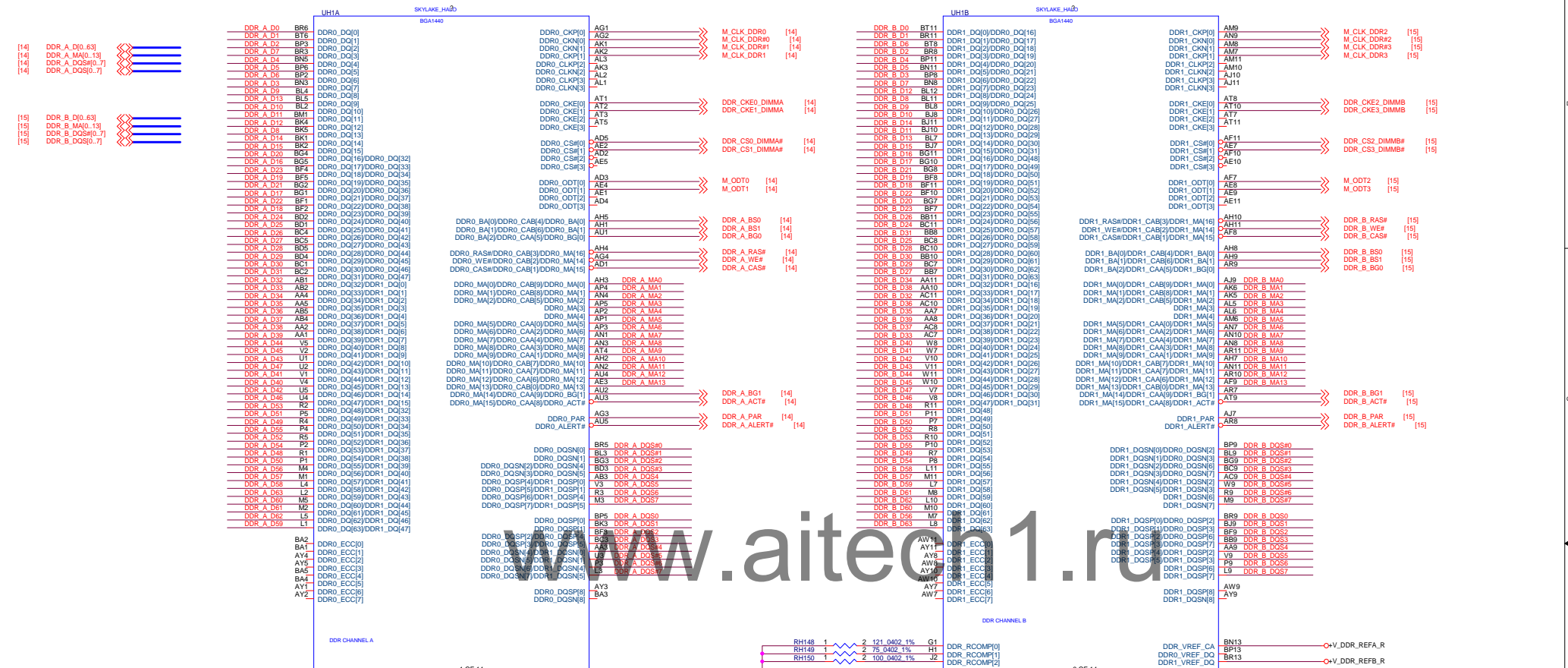
[23] PEG_HTX_C_GRX_P10_15] << PEG_HTX_C_GRX_P10_15]
[23] PEG_HTX_C_GRX_N10_15] << PEG_HTX_C_GRX_N10_15]
[23] PEG_GTX_C_HRX_P10_15] >> PEG_GTX_C_HRX_P10_15]
[23] PEG_GTX_C_HRX_N10_15] >> PEG_GTX_C_HRX_N10_15]



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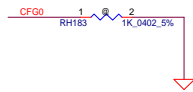
Interleave



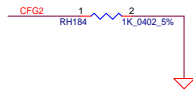
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				<i>PROCESSOR(3/7) DDRIII</i>	
				Size	Document Number
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CFG Straps for Processor

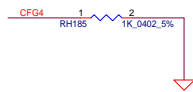
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	<p>* 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



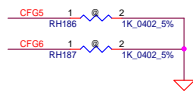
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>* 0: Lane Reversed</p>



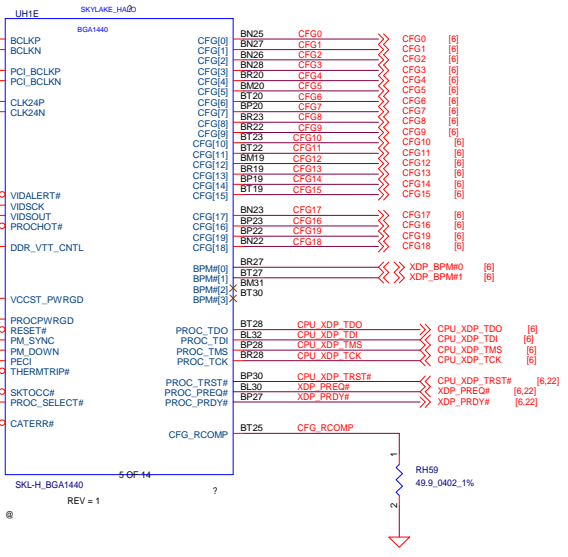
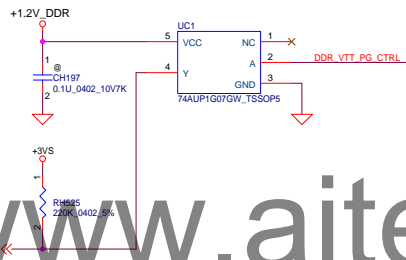
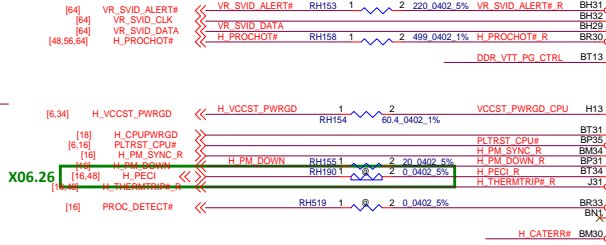
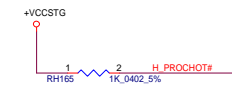
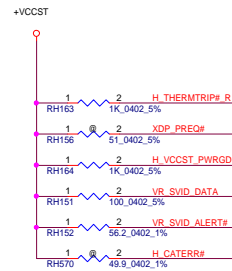
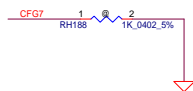
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

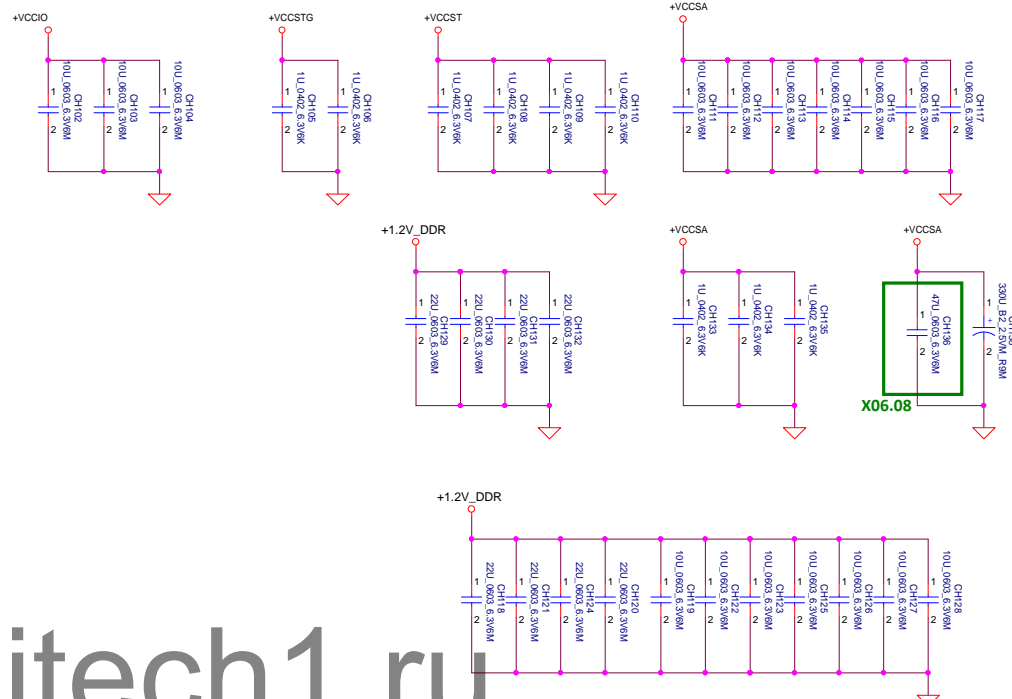


PCIe Port Bifurcation Straps	
CFG[6:5]	<p>* 11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>

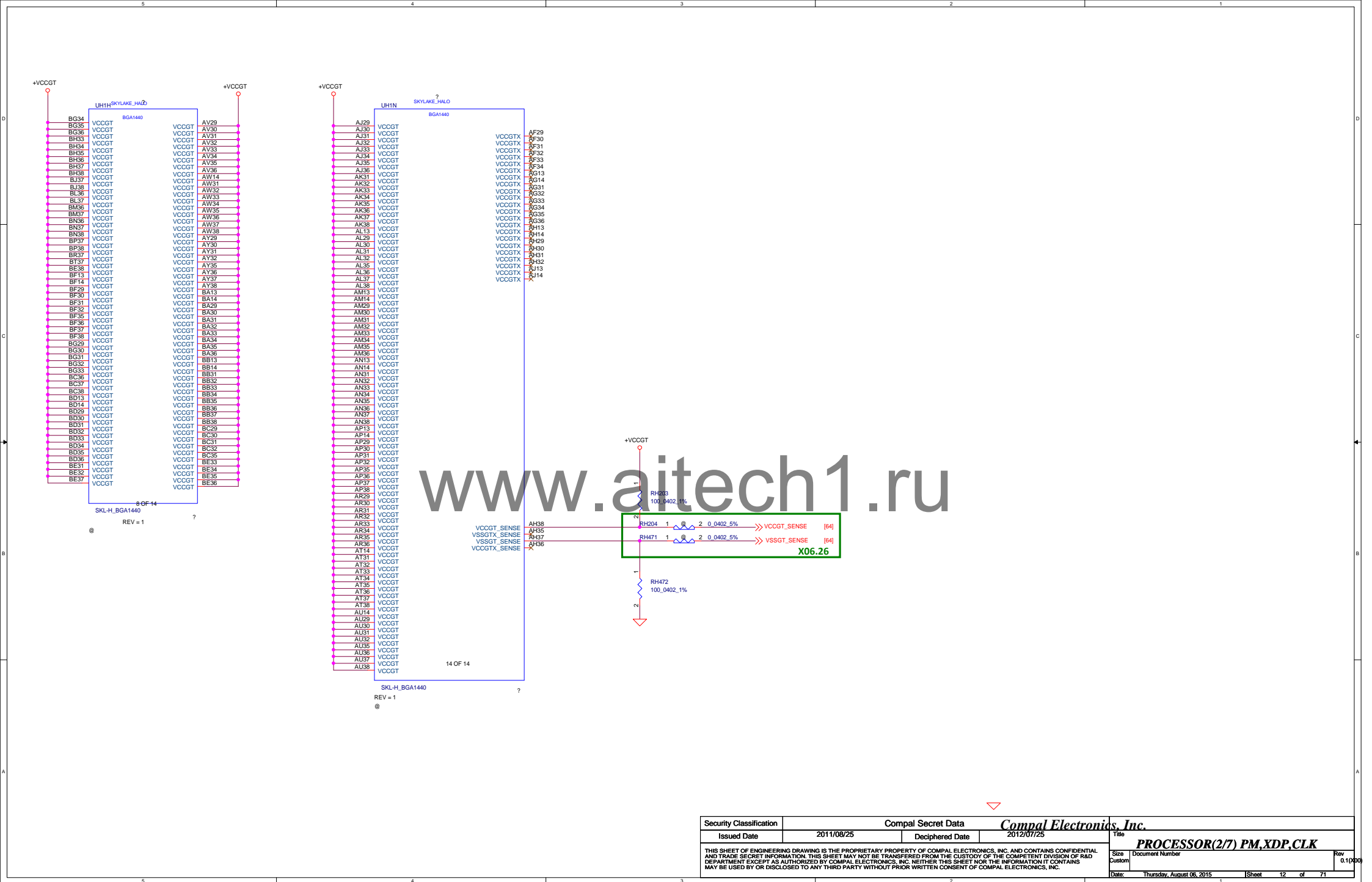


PEG DEFER TRAINING	
CFG7	<p>* 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

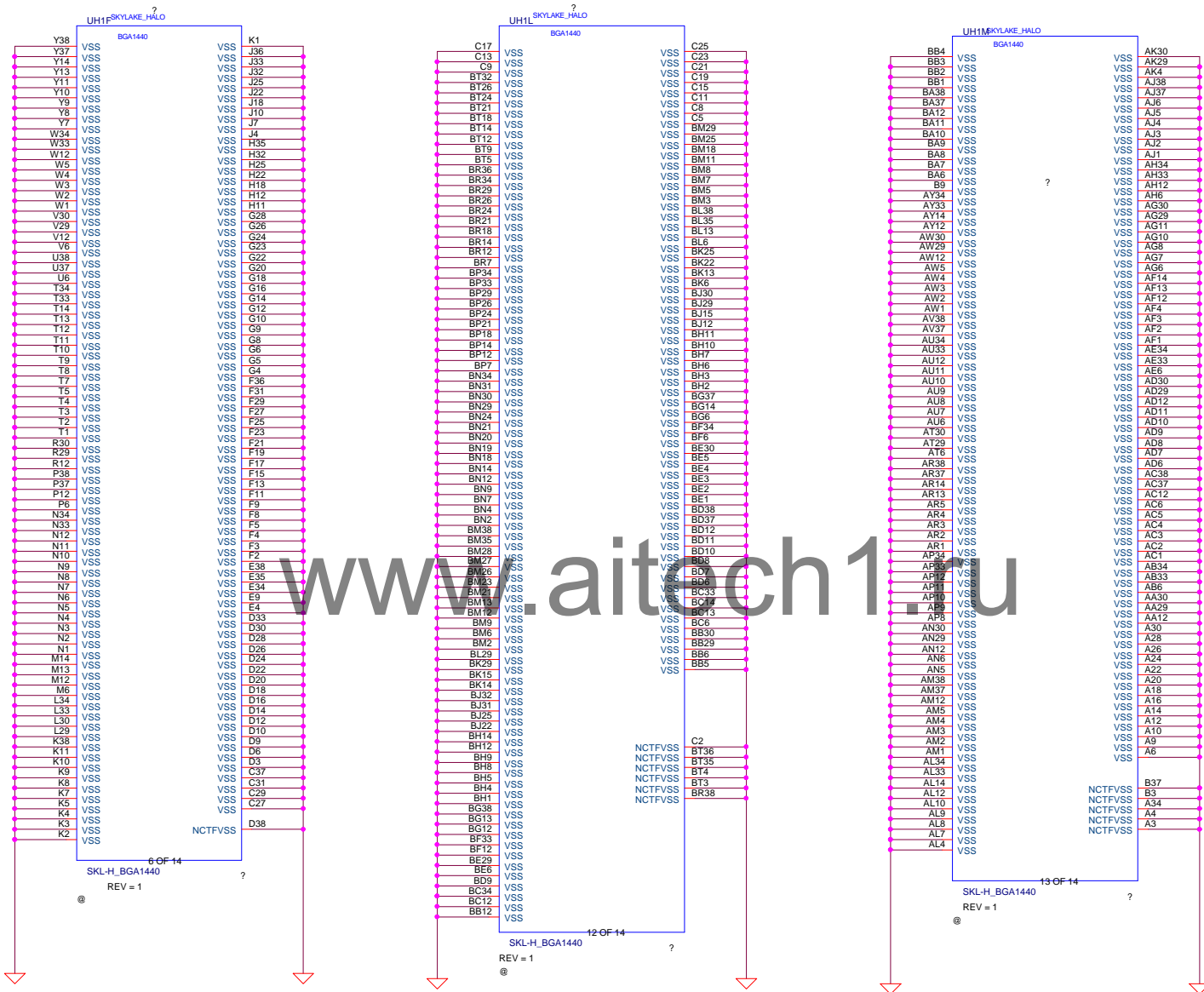




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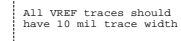


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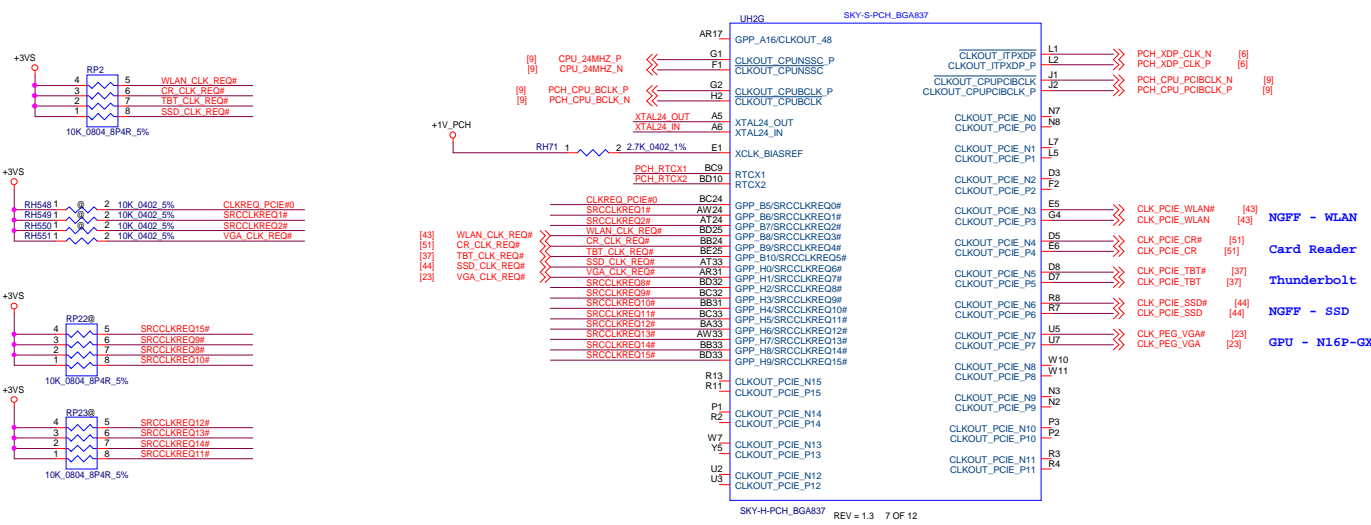


The circuit diagram shows a 5-bit DAC implemented with a 0.6V voltage source and five resistors. The resistors are labeled CD12, CD13, CD14, CD15, and CD16, each with a value of 100.0000 and a tolerance of 0.5000M. The resistors are connected in a ladder configuration to the positive terminal of the 0.6V source. The negative terminal of the source is connected to ground, indicated by a triangle symbol.

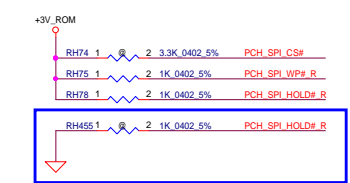
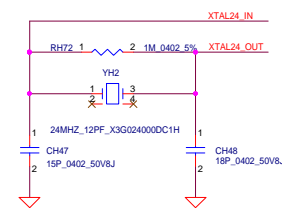
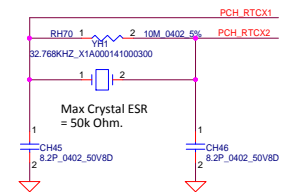
The schematic diagram illustrates the power supply section of the TMS320C6701 evaluation board. It features two +1.2V_DDR power planes. The top plane is connected to a +1.2V input and contains eight decoupling capacitors (CD18 to CD25) in parallel. The bottom plane is connected to a +1.2V input and contains eight decoupling capacitors (CD26 to CD33) in parallel. A CD11 capacitor is also shown connected between the two planes.



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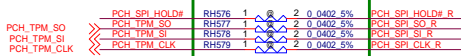
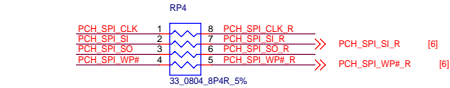


RTC CRYSTAL

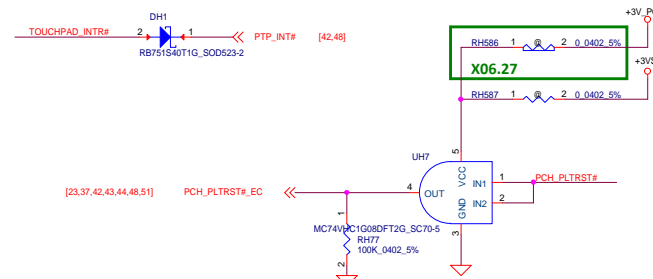
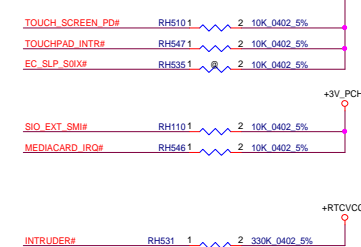
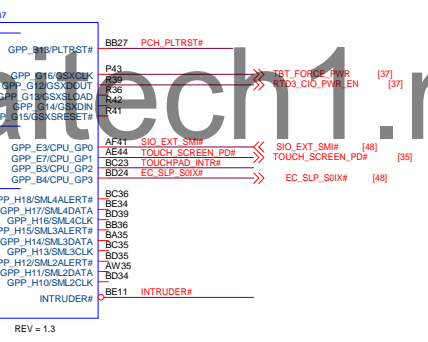
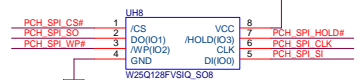


9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

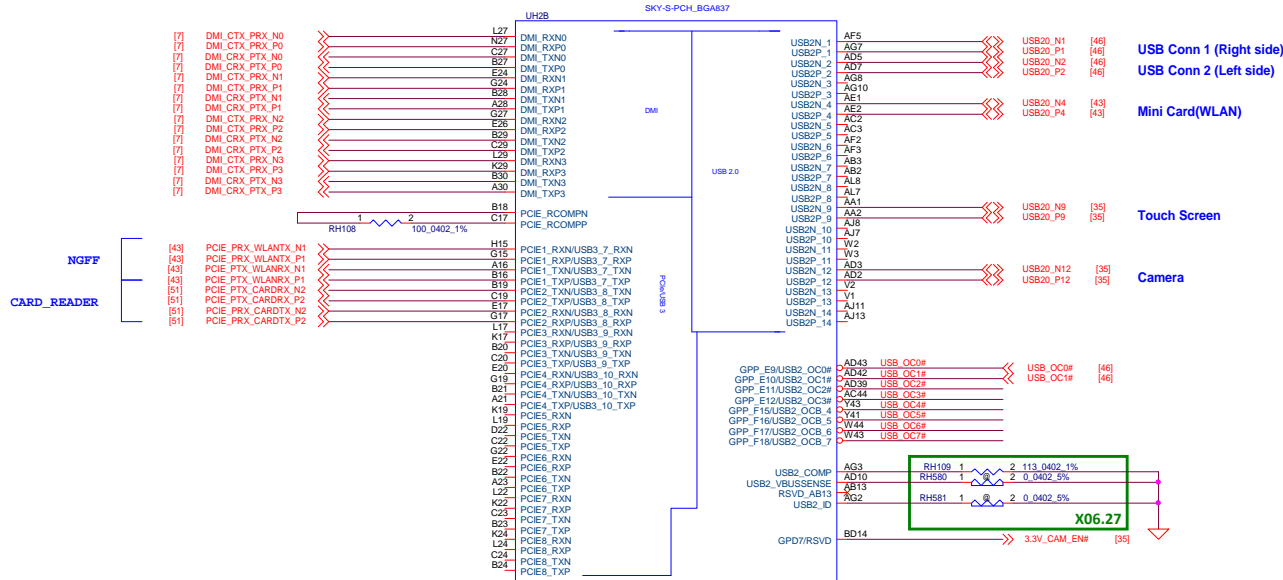
Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-E51/E51 samples.



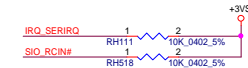
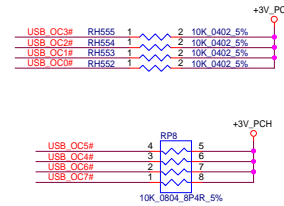
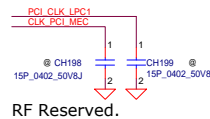
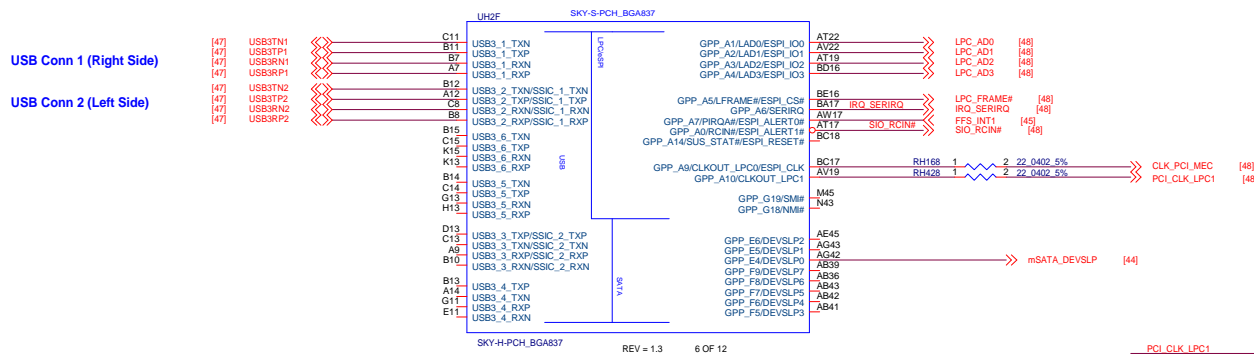
SPI ROM FOR ME (16MByte)



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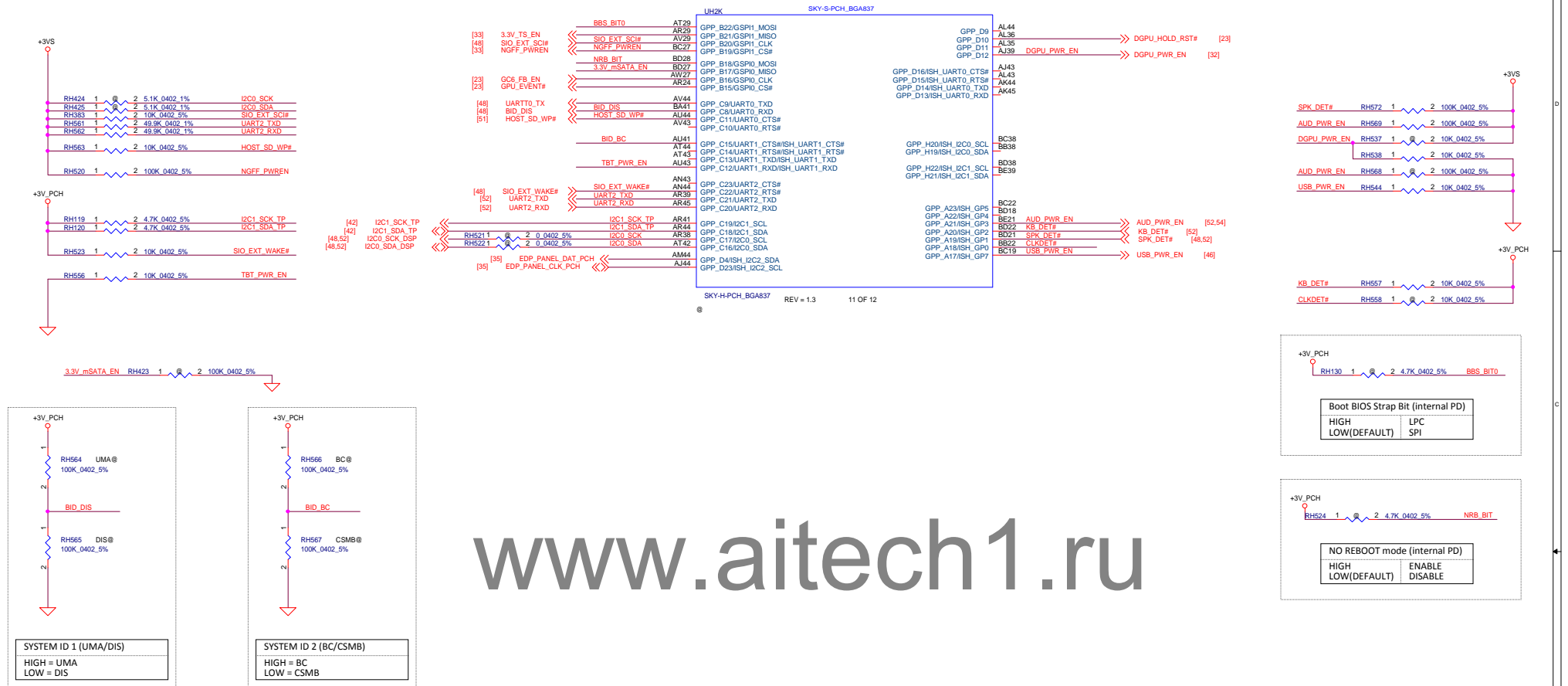


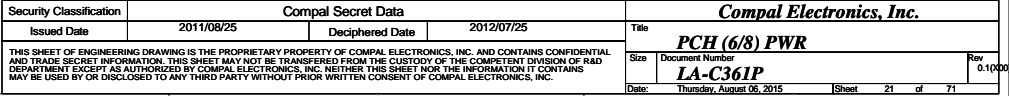
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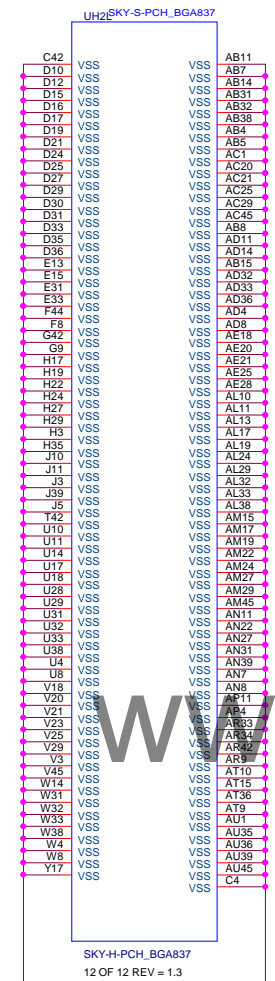


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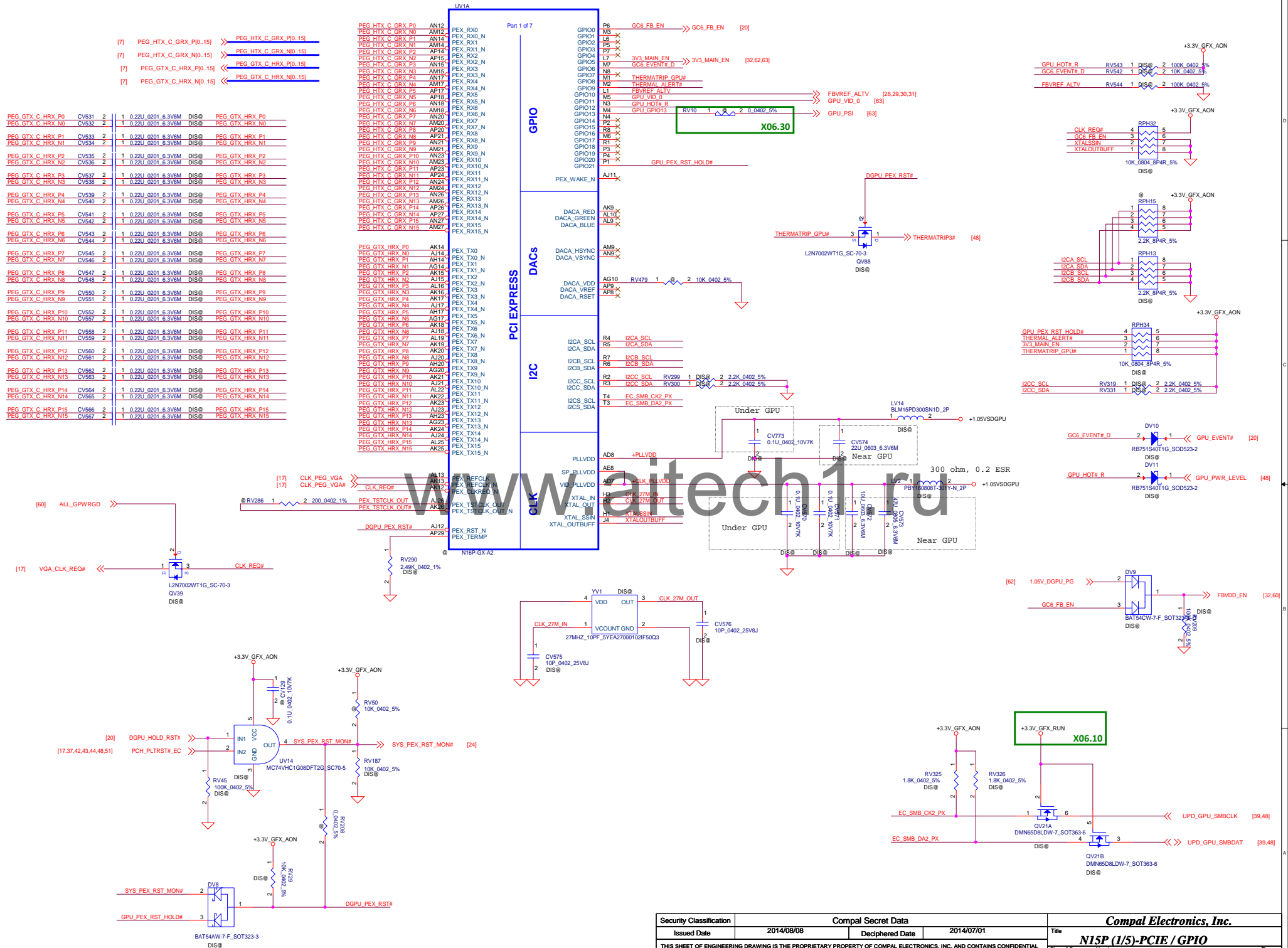
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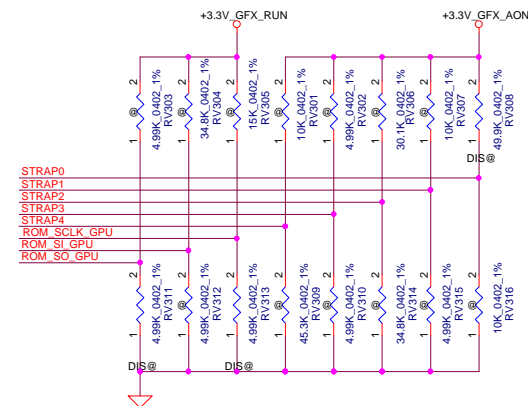
Table 15-2. Resistance Mapping to Hex Values

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

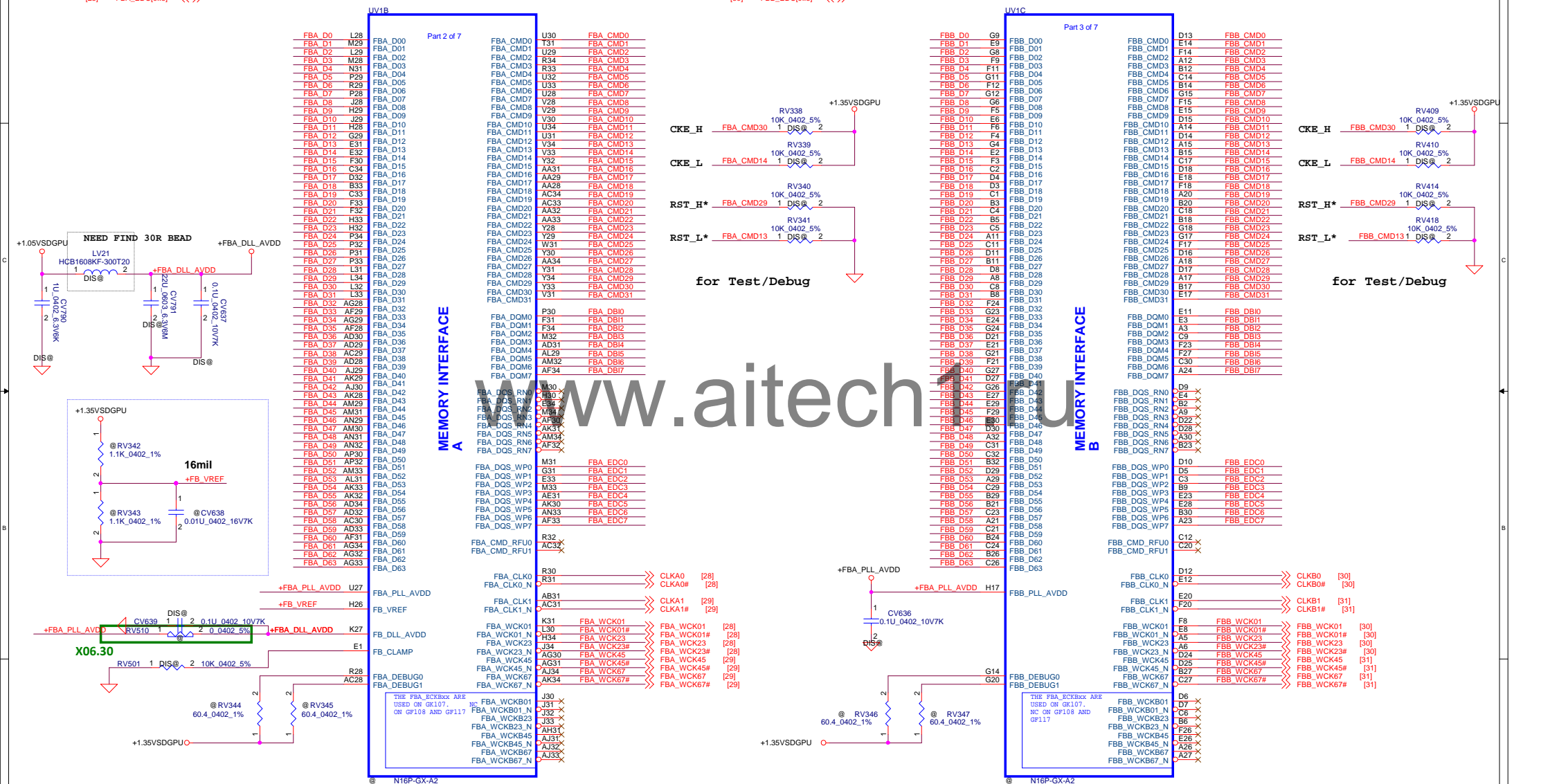
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				Date: Thursday, August 06, 2015	Sheet 26 of 71

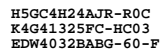
[28] FBA_D[0..31] <<> FBA_D[0..31]
[29] FBA_D[32..63] <<> FBA_D[32..63]
[28,29] FBA_CMD[0..31] <<> FBA_CMD[0..31]
[29] FBA_DB[4..7] <<> FBA_DB[4..7]
[28] FBA_DB[0..3] <<> FBA_DB[0..3]
[29] FBA_EDC[4..7] <<> FBA_EDC[4..7]
[28] FBA_EDC[0..3] <<> FBA_EDC[0..3]

[30] FBB_D[0..31] <<> FBB_D[0..31]
[31] FBB_D[32..63] <<> FBB_D[32..63]
[30,31] FBB_CMD[0..31] <<> FBB_CMD[0..31]
[31] FBB_DB[4..7] <<> FBB_DB[4..7]
[30] FBB_DB[0..3] <<> FBB_DB[0..3]
[31] FBB_EDC[4..7] <<> FBB_EDC[4..7]
[30] FBB_EDC[0..3] <<> FBB_EDC[0..3]



64X32 GDDR5

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RS5*	CMD28	RS5*
CMD13	RS1*	CMD29	RS1*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

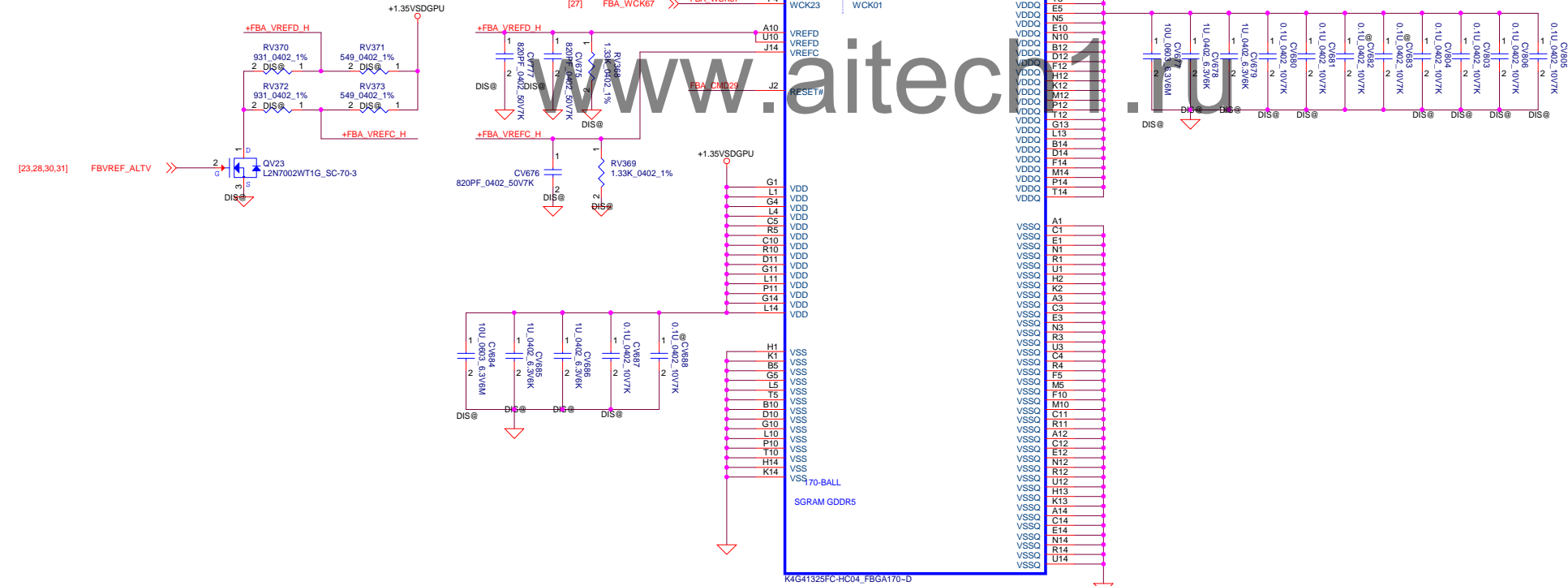


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Title		VRAM_GDDR5_A Lower	
Size	Document Number	Rev 0.1(00)	
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Memory Partition A - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0...31	GB2-64, GB4-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



64X32 GDDR5

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	R5T*	CMD29	R5T*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

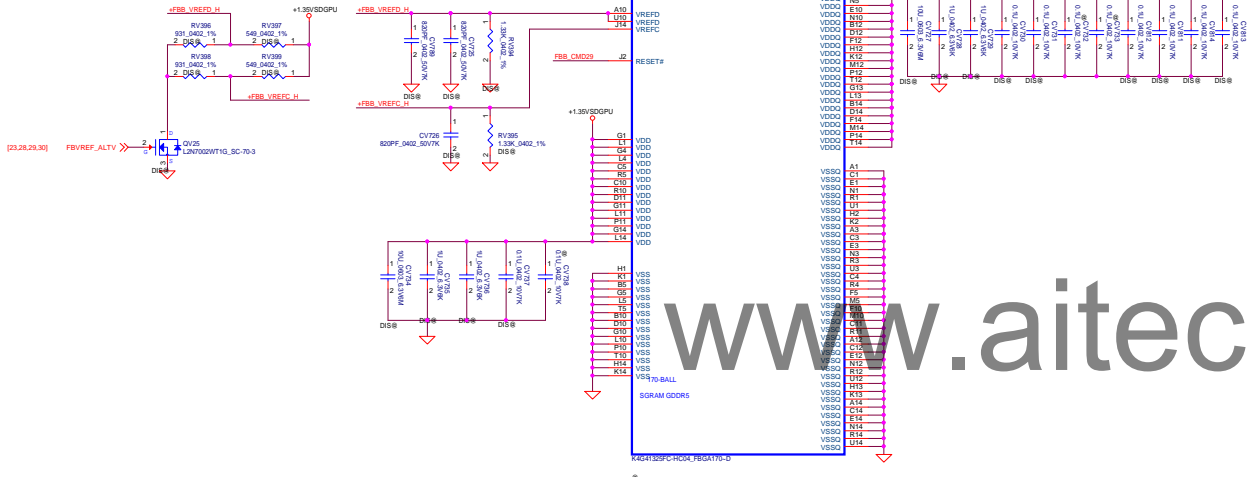


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Memory Partition B - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

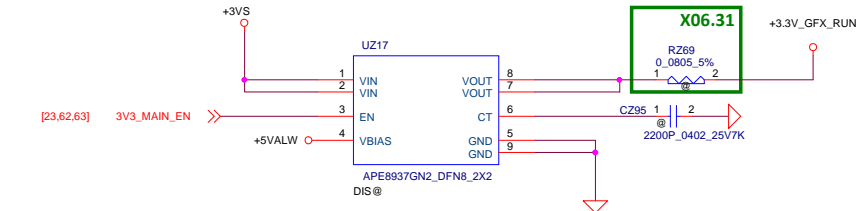
GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CM00	C5*	CM016	C5*
CM01	A3, B43	CM017	A3, B43
CM02	A2, B40	CM018	A2, B40
CM03	A4, B42	CM019	A4, B42
CM04	A5, B41	CM020	A5, B41
CM05	WE*	CM021	WE*
CM06	A7, A8	CM022	A7, A8
CM07	A8, A11	CM023	A8, A11
CM08	AB*	CM024	AB*
CM09	A12, RFU	CM025	A12, RFU
CM010	AD, A10	CM026	AD, A10
CM011	A1, A9	CM027	A1, A9
CM012	RA*	CM028	RA*
CM013	RS*	CM029	RS*
CM014	CR*	CM030	CR*
CM015	CA*	CM031	CA*



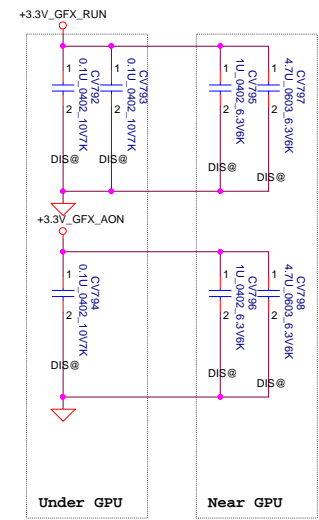
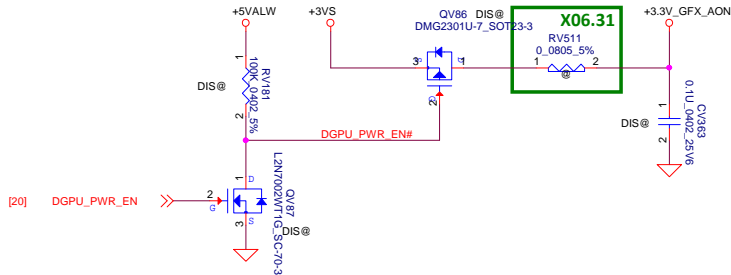
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				New 0.100	
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+3.3V_GFX_RUN



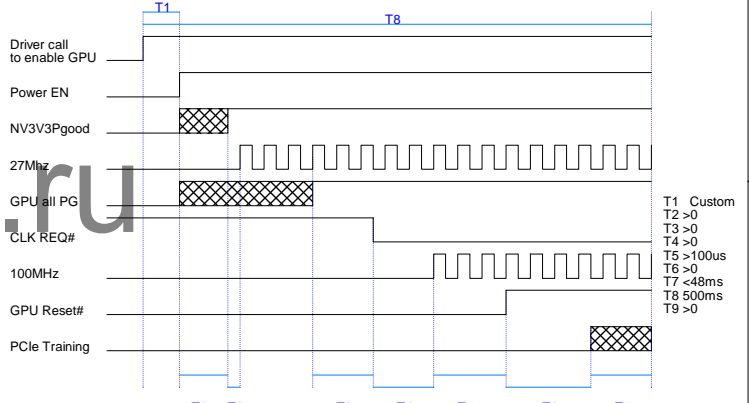
+3VALW to +3.3V_GFX_AON



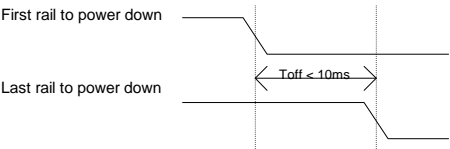
GPU Power Up Power Rail Sequence



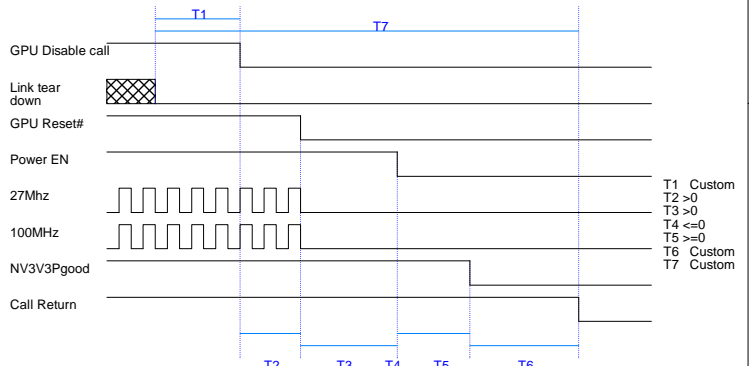
GPU Power Up Sub-system Sequence



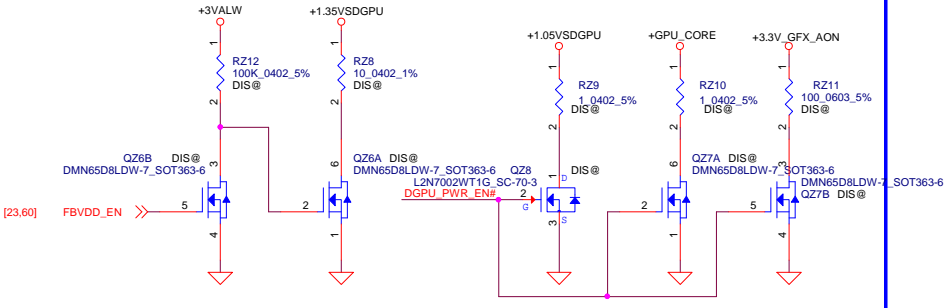
GPU Power Down Sequence



GPU Power Down Sub-system Sequence

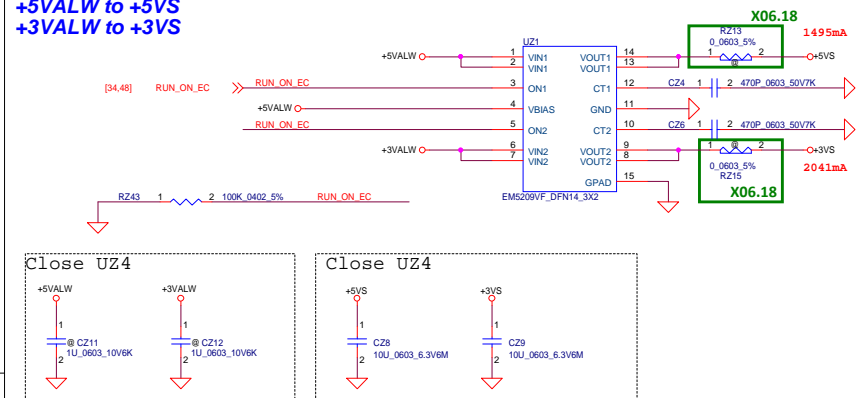


Discharge

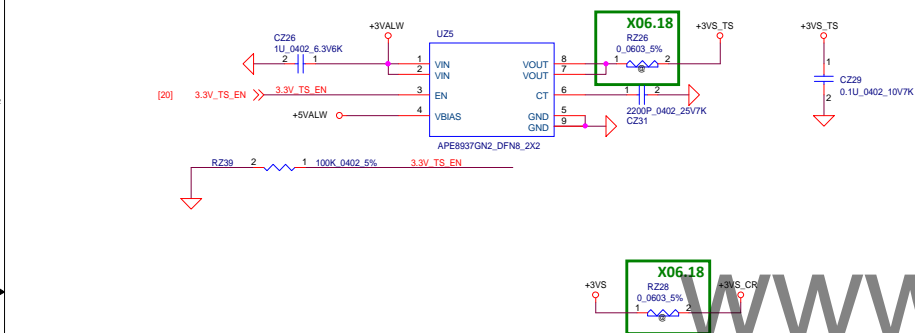


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Date: Thursday, August 06, 2015					Sheet 32 of 71

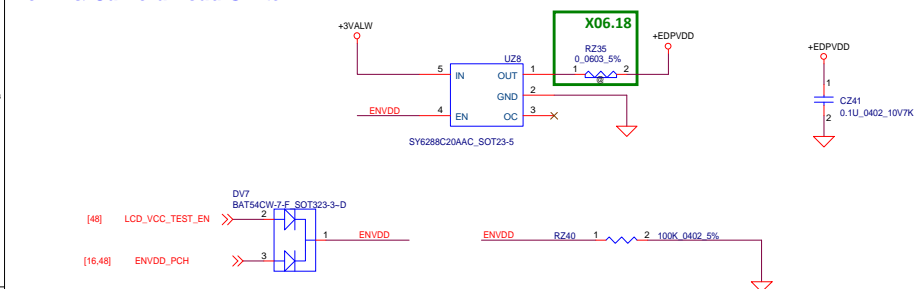
+5VALW to +5VS
+3VALW to +3VS



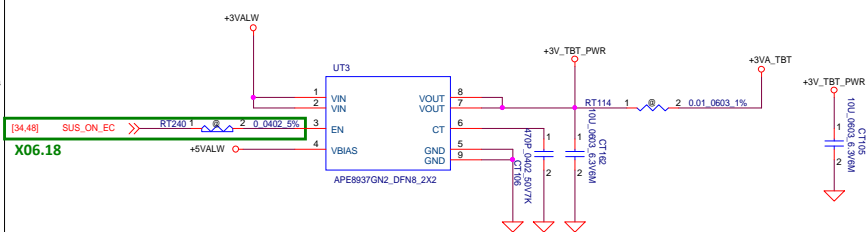
Touch Screen Load Switch & Card Reader



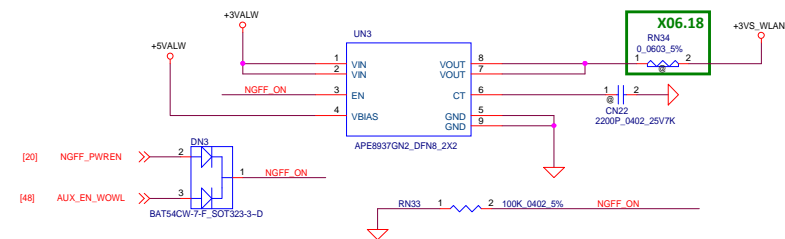
eDP & Camera Load Switch



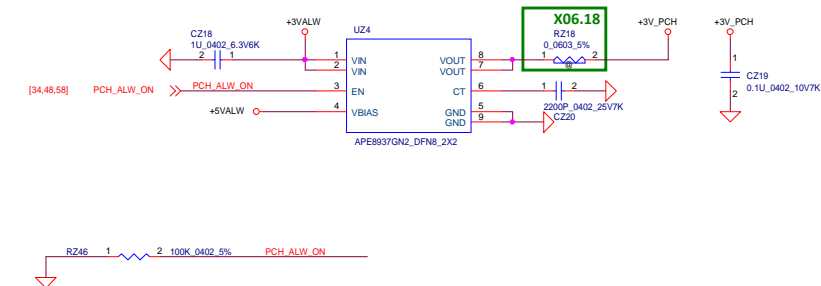
Alpine Ridge(TBT) Load Switch



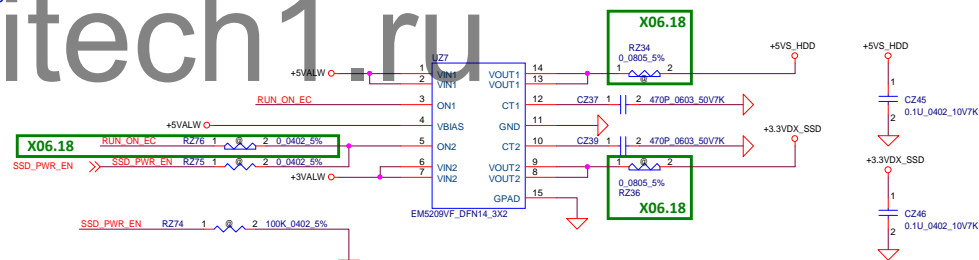
WLAN Load Switch



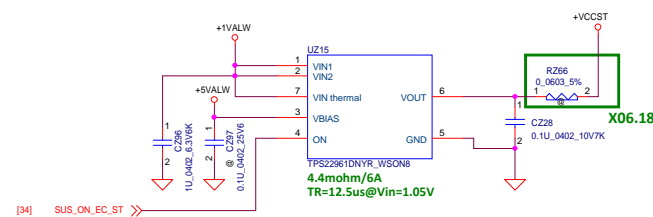
+3VALW to +3V_PCH



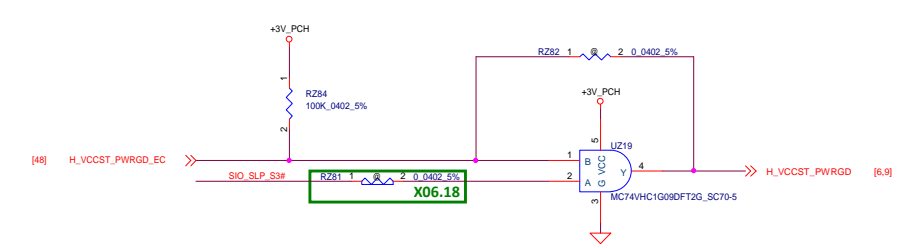
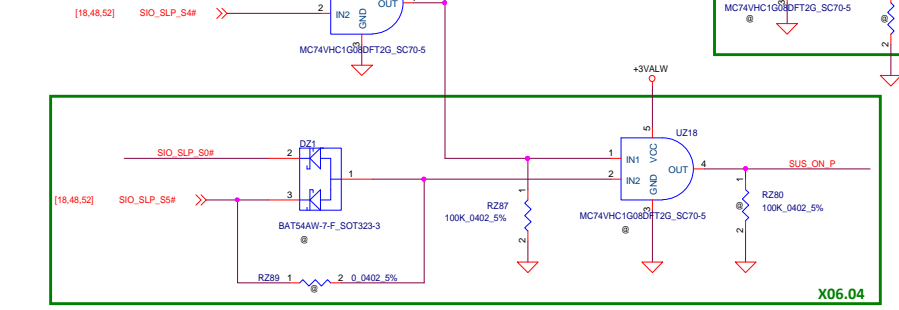
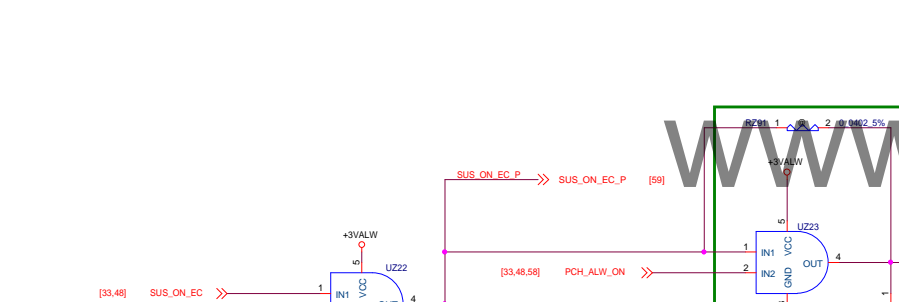
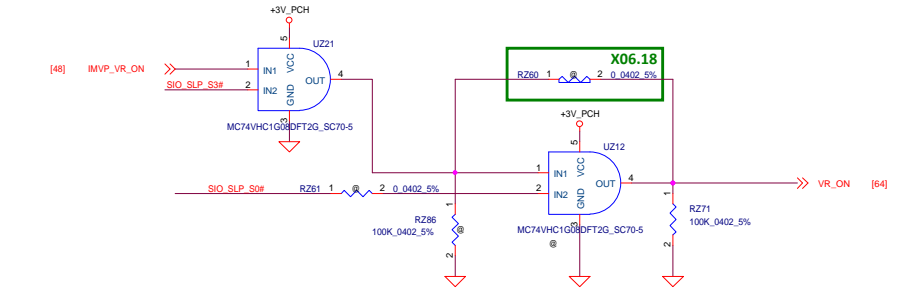
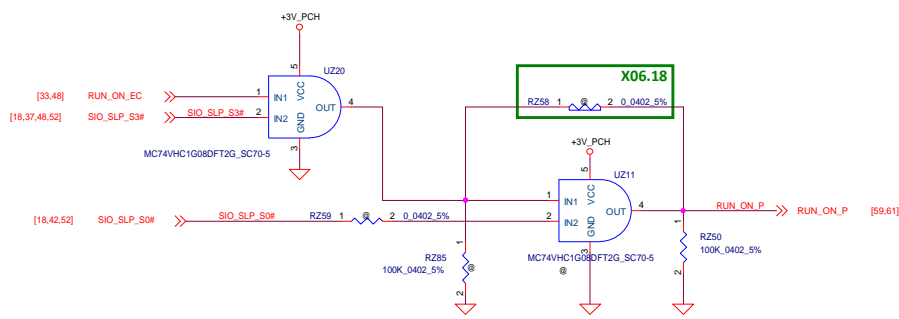
HDD, SSD Load Switch



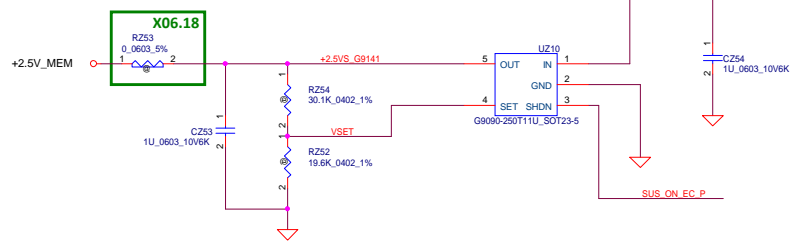
+VCCST Load Switch



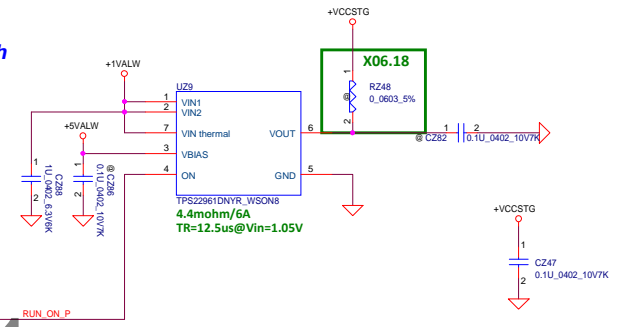
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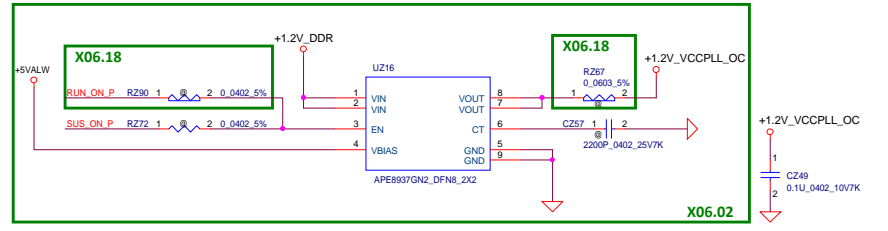
DDR4 VPP Load Switch



+VCCSTG Load Switch



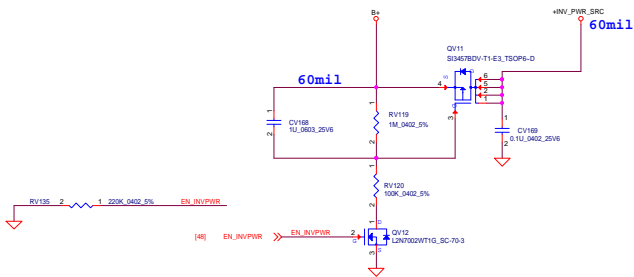
+VCCPLL_OC Load Switch



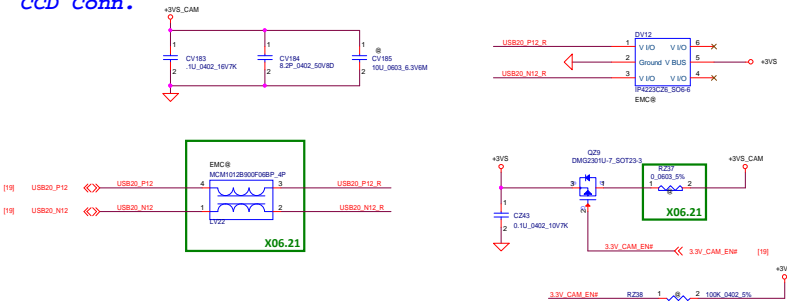
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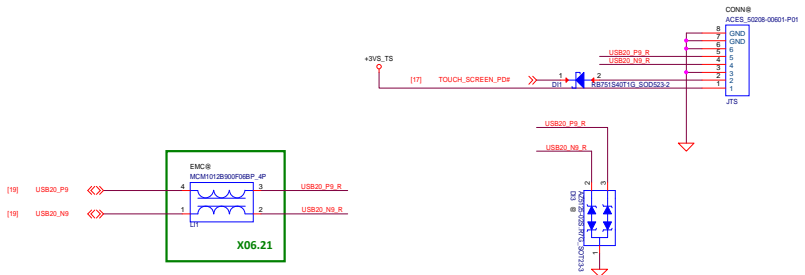
LCD backlight PWR CTRL



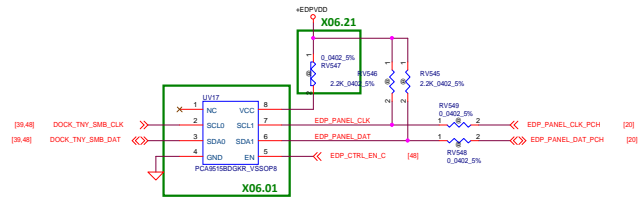
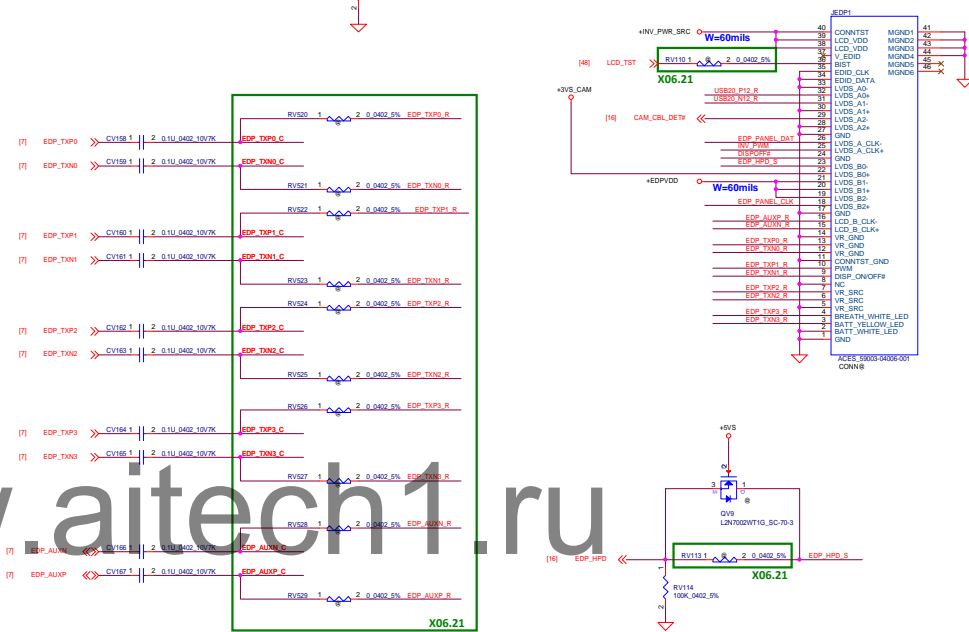
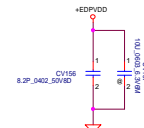
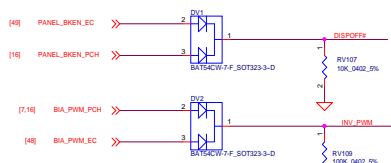
CCD Conn.



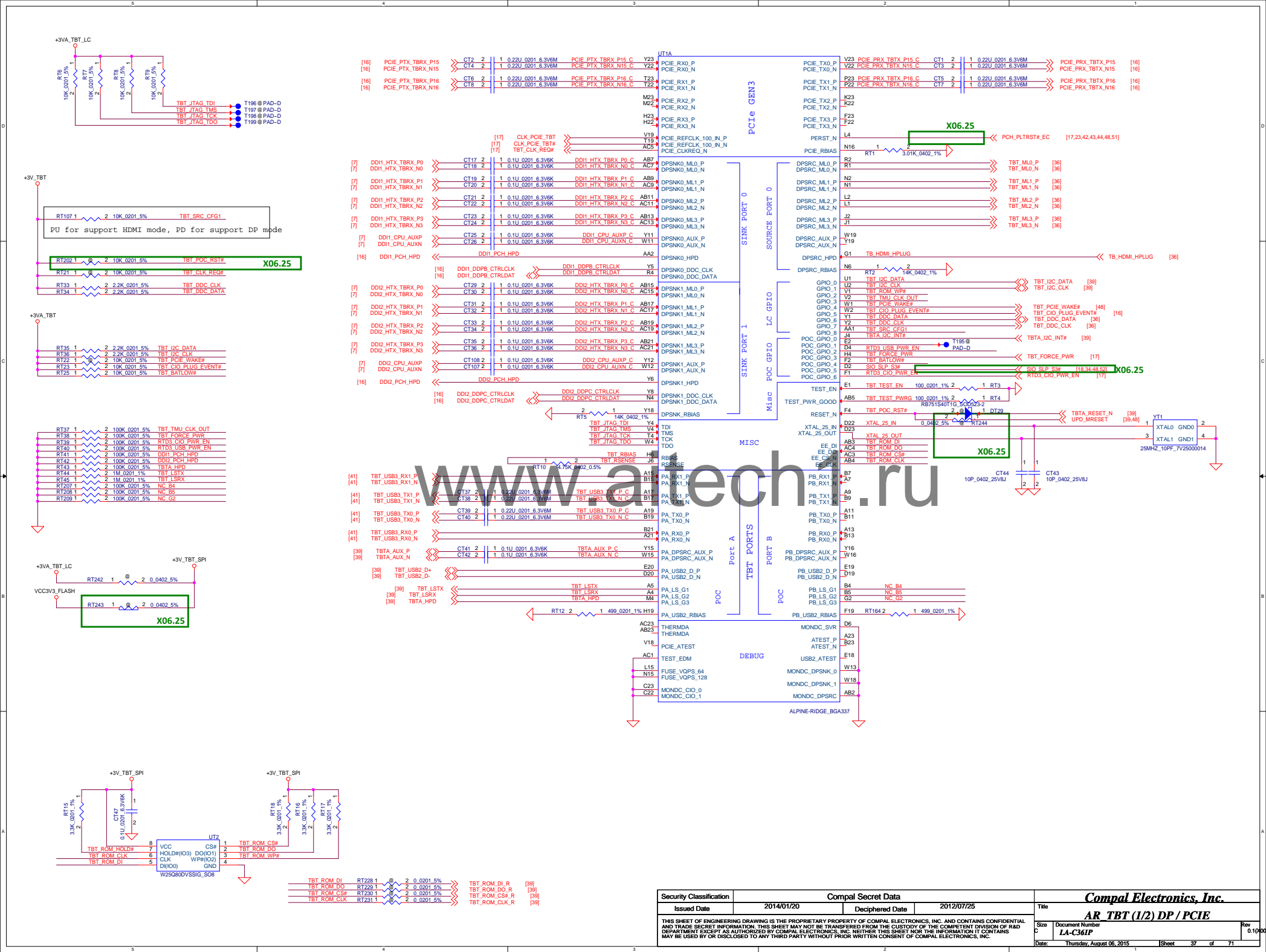
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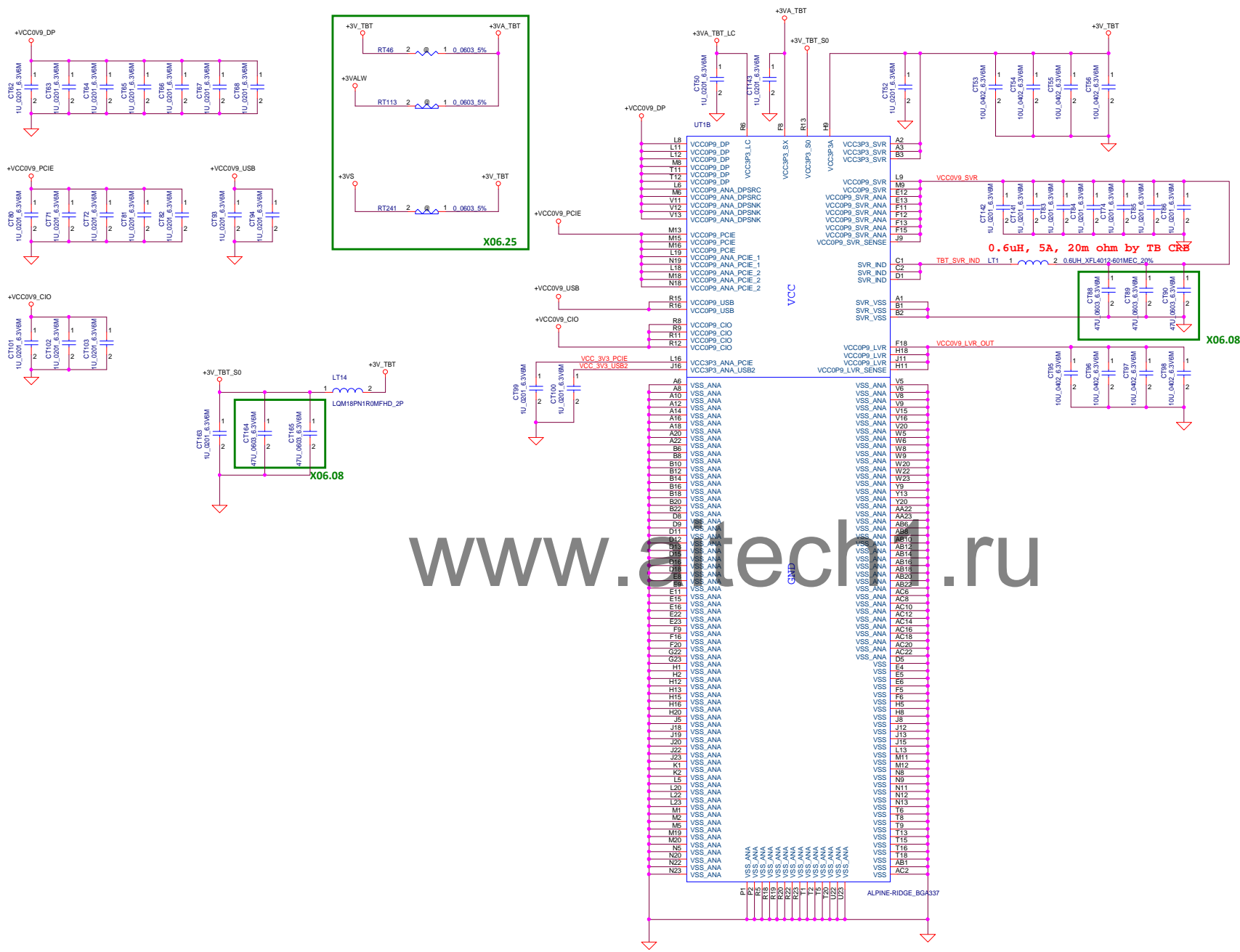


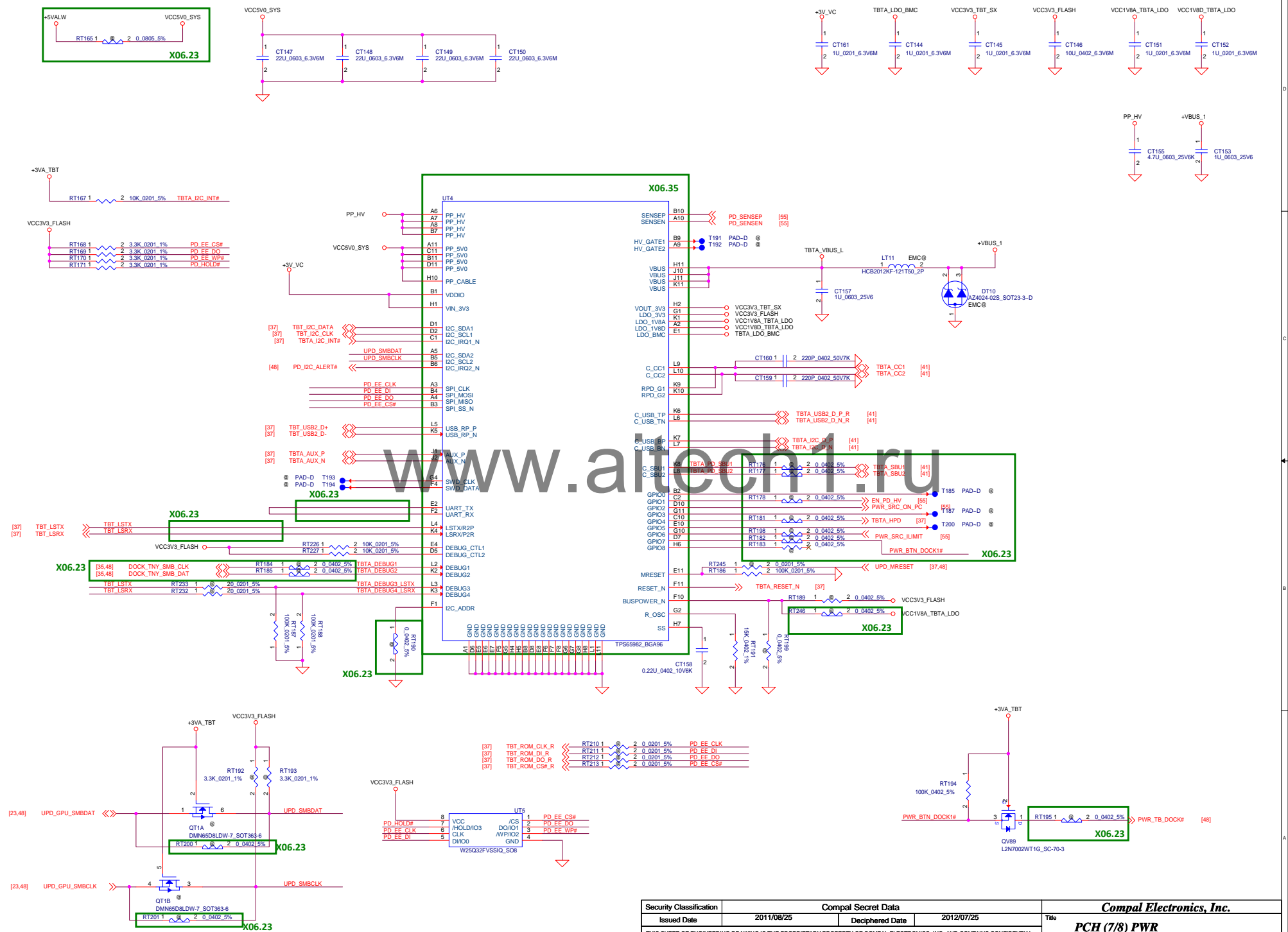
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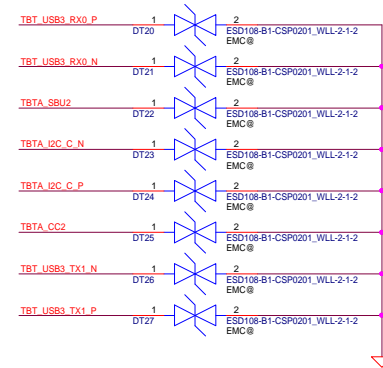
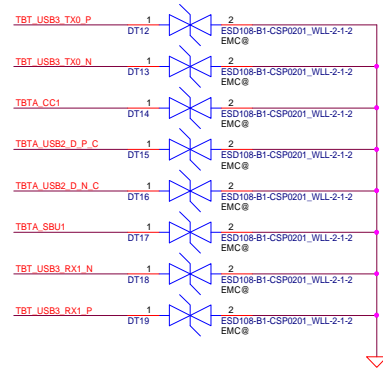
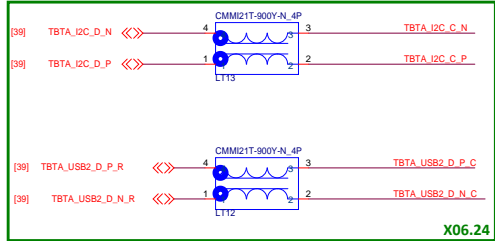


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						LA-C361P
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						01/000

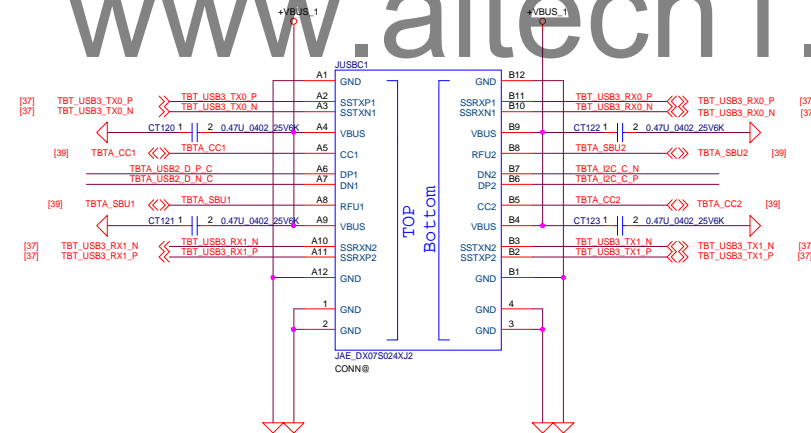
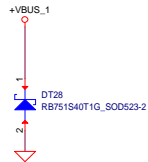
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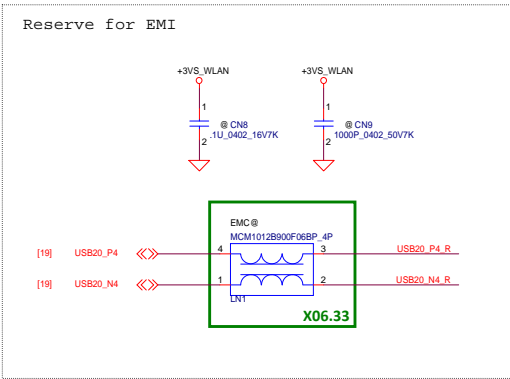
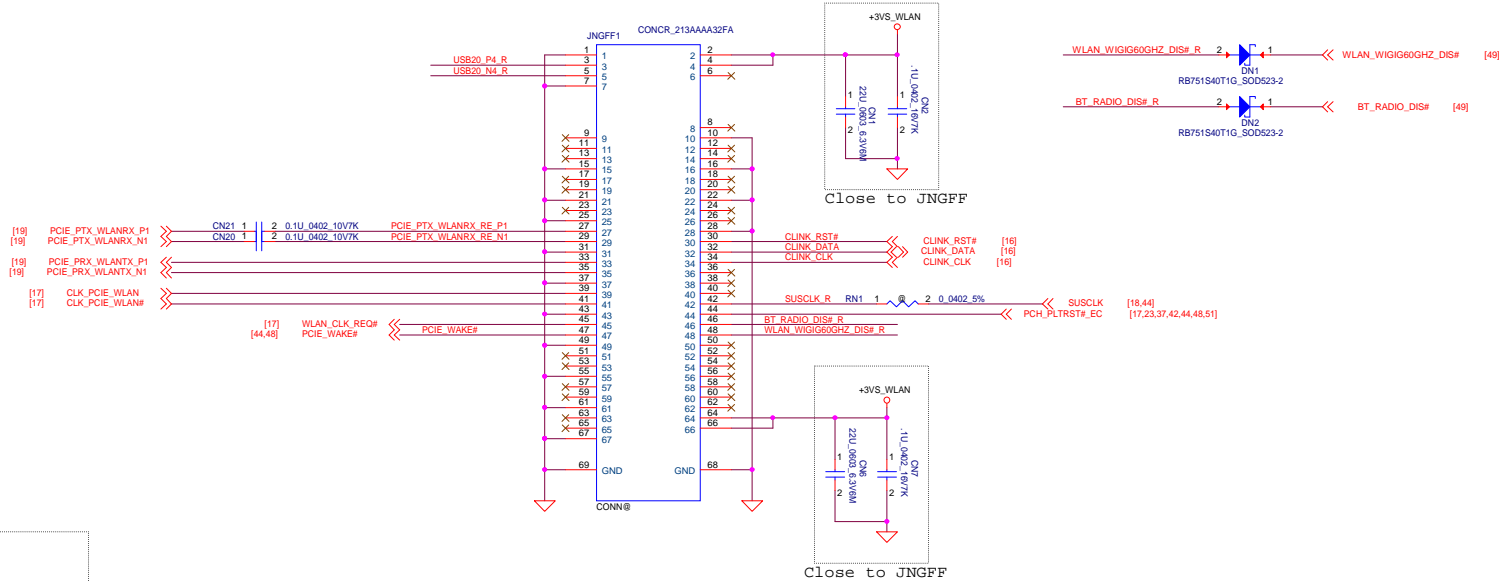


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Date: Thursday, August 06, 2015				Sheet 41	Rev 0.1(00)

M.2 Slot-A Key-A (WLAN + BT)

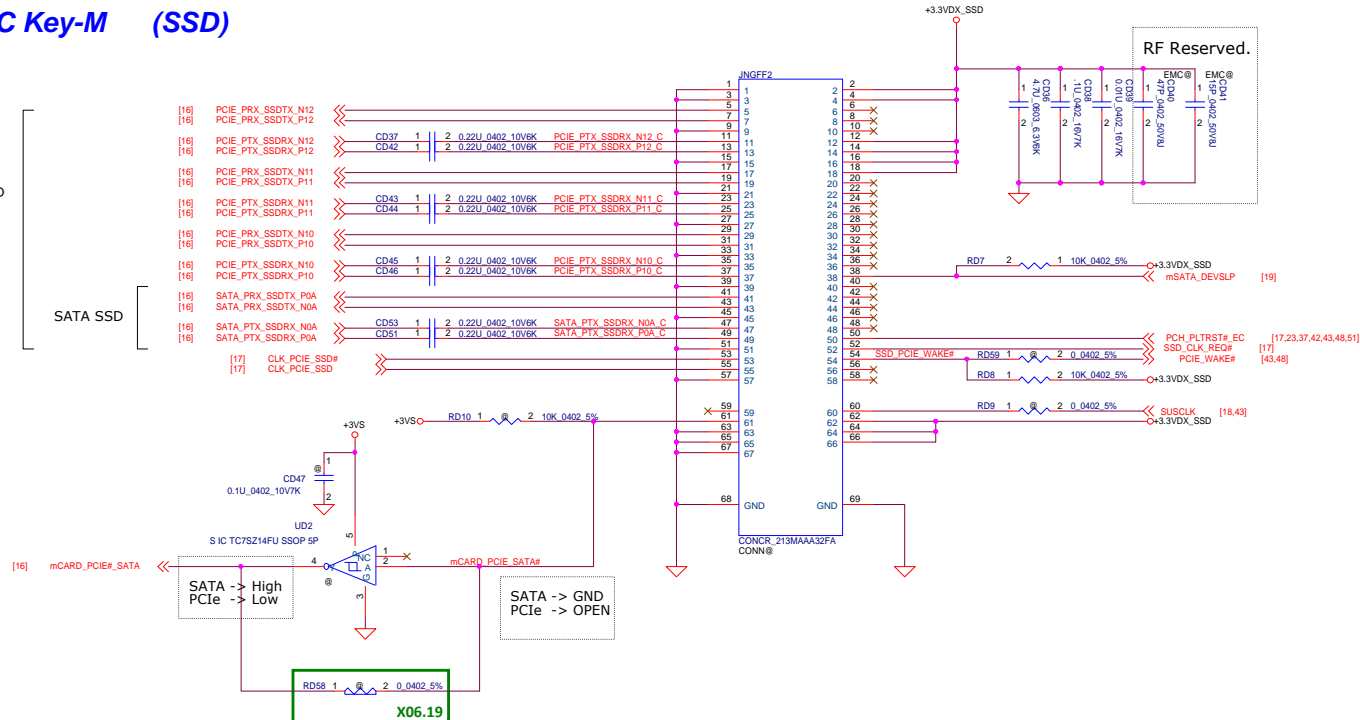


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M.2 Slot-C Key-M (SSD)

PCIe SSD

SATA SSD

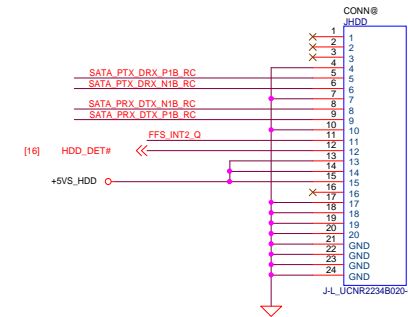


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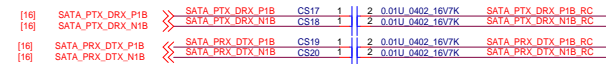
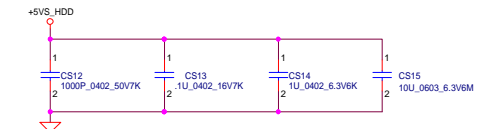
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2011/08/25		2012/07/25		SSD	
Size		Document Number		Rev	
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HDD CONN

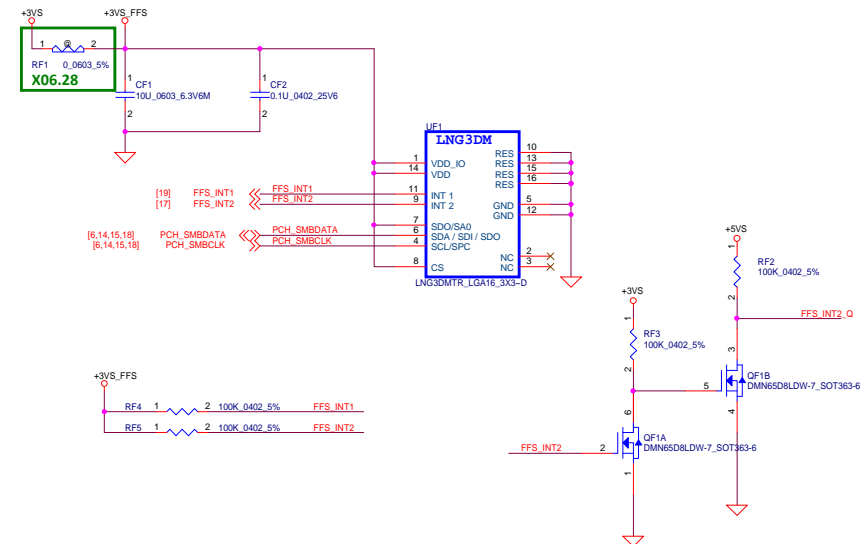


Place near HDD CONN (JHDD1)



BYPASS Circuit

Free Fall Sensor

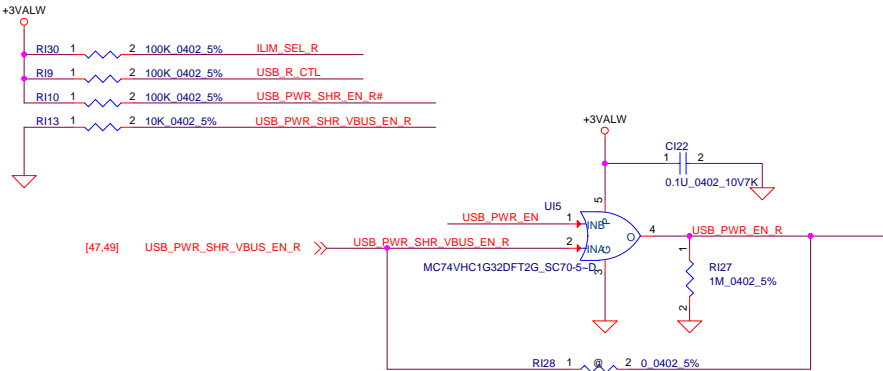


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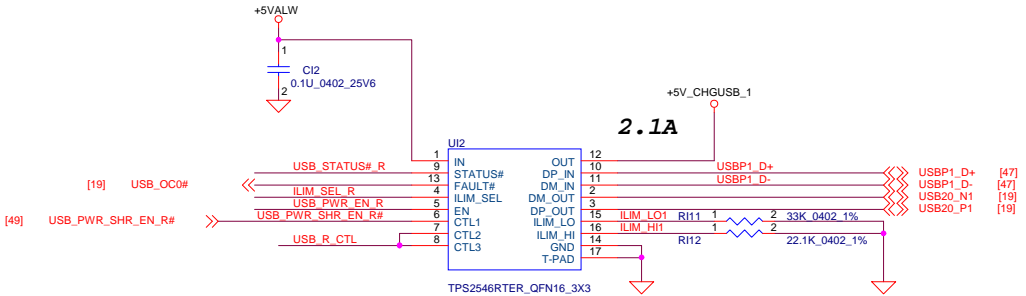
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

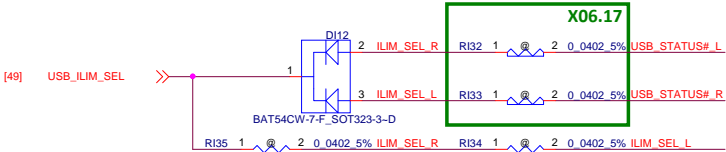
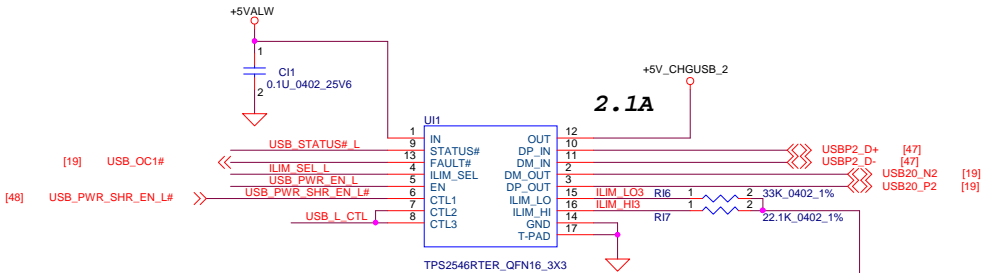
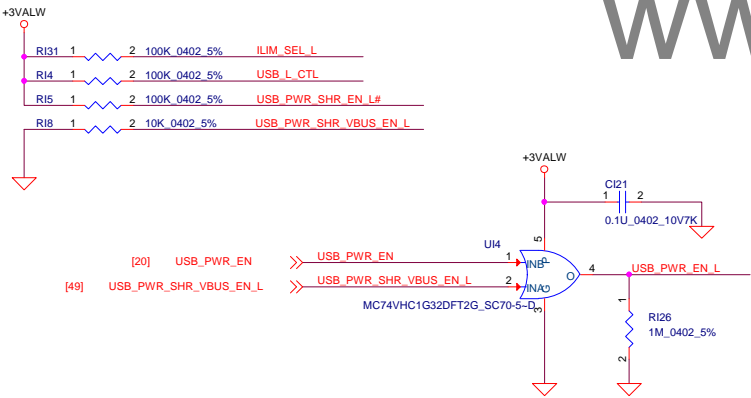


USB3.0 / USB2.0 Port1 (Right Side)

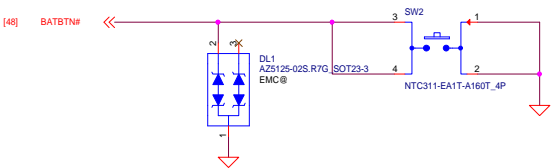


USB3.0 / USB2.0 Port2 (Left Side)

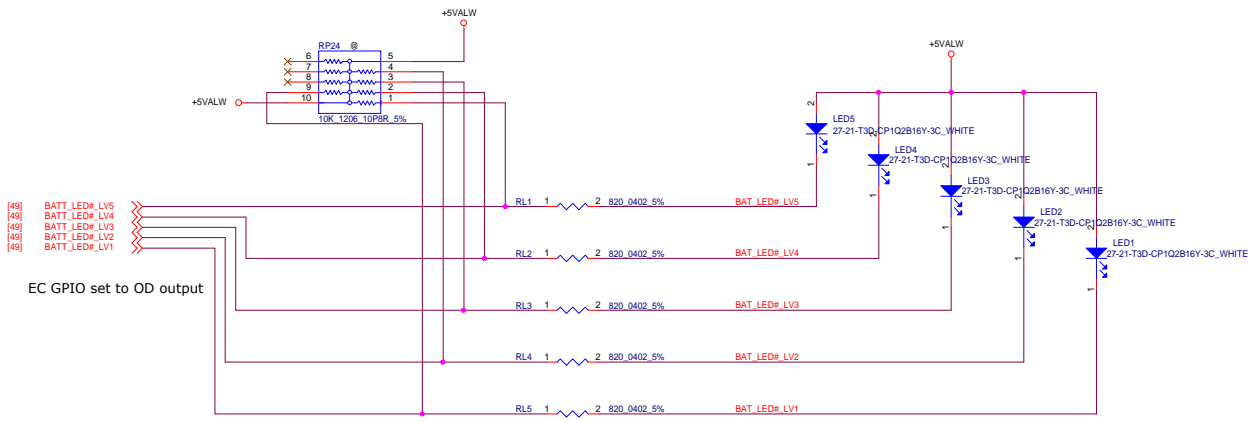
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BATT LED Power Button



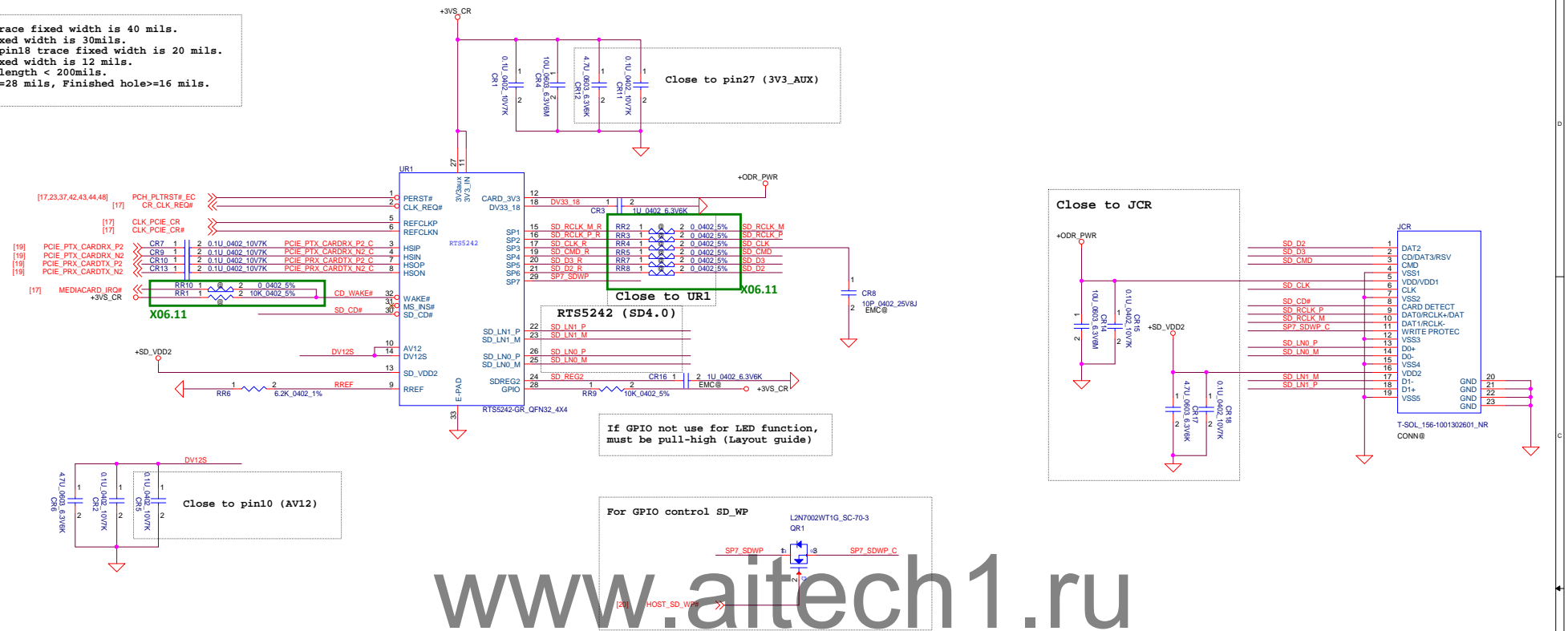
Battery Gauge LED



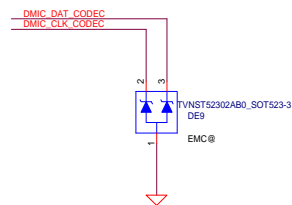
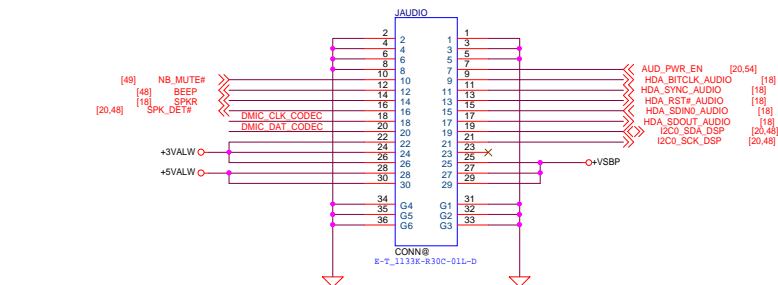
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Card Reader

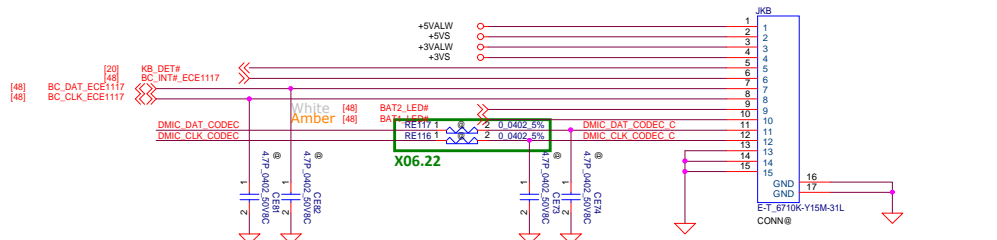
Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.



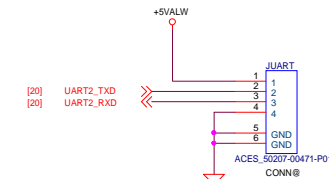
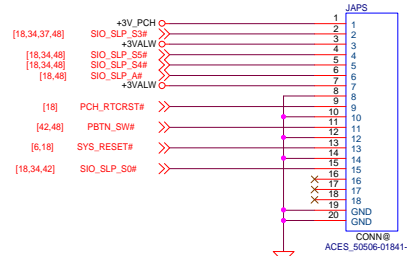
AUDIO Board Conn.



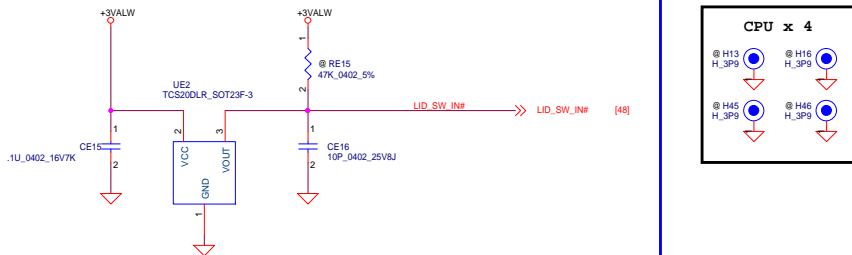
Keyboard Controller board + DMIC



APS CONN

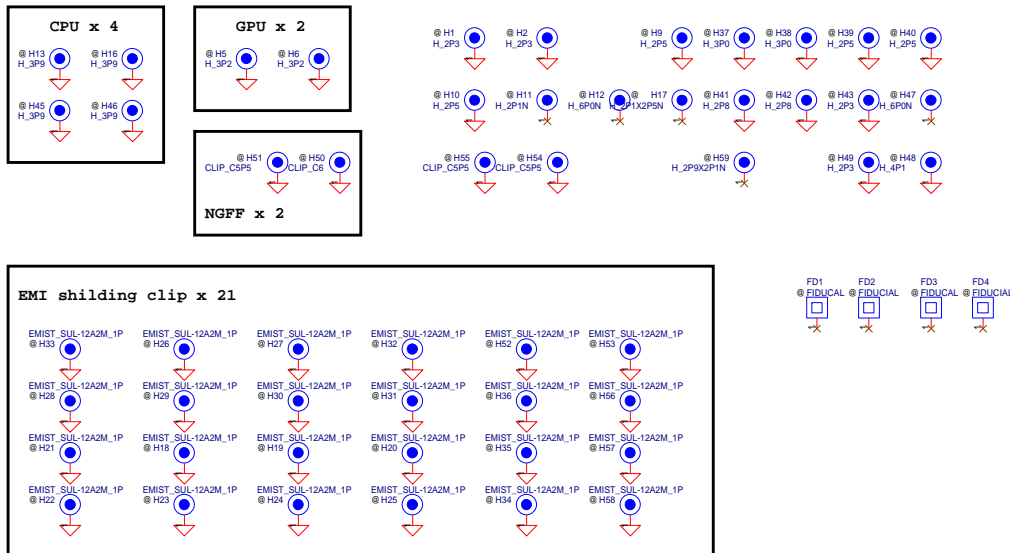


Lid Switch

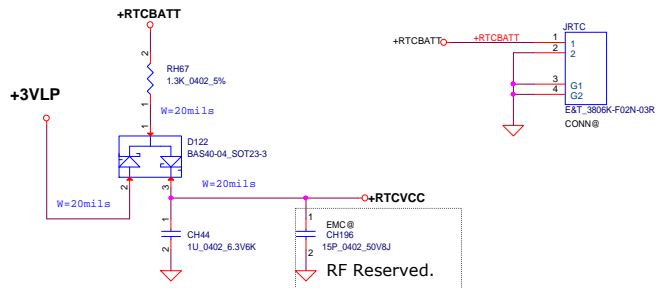


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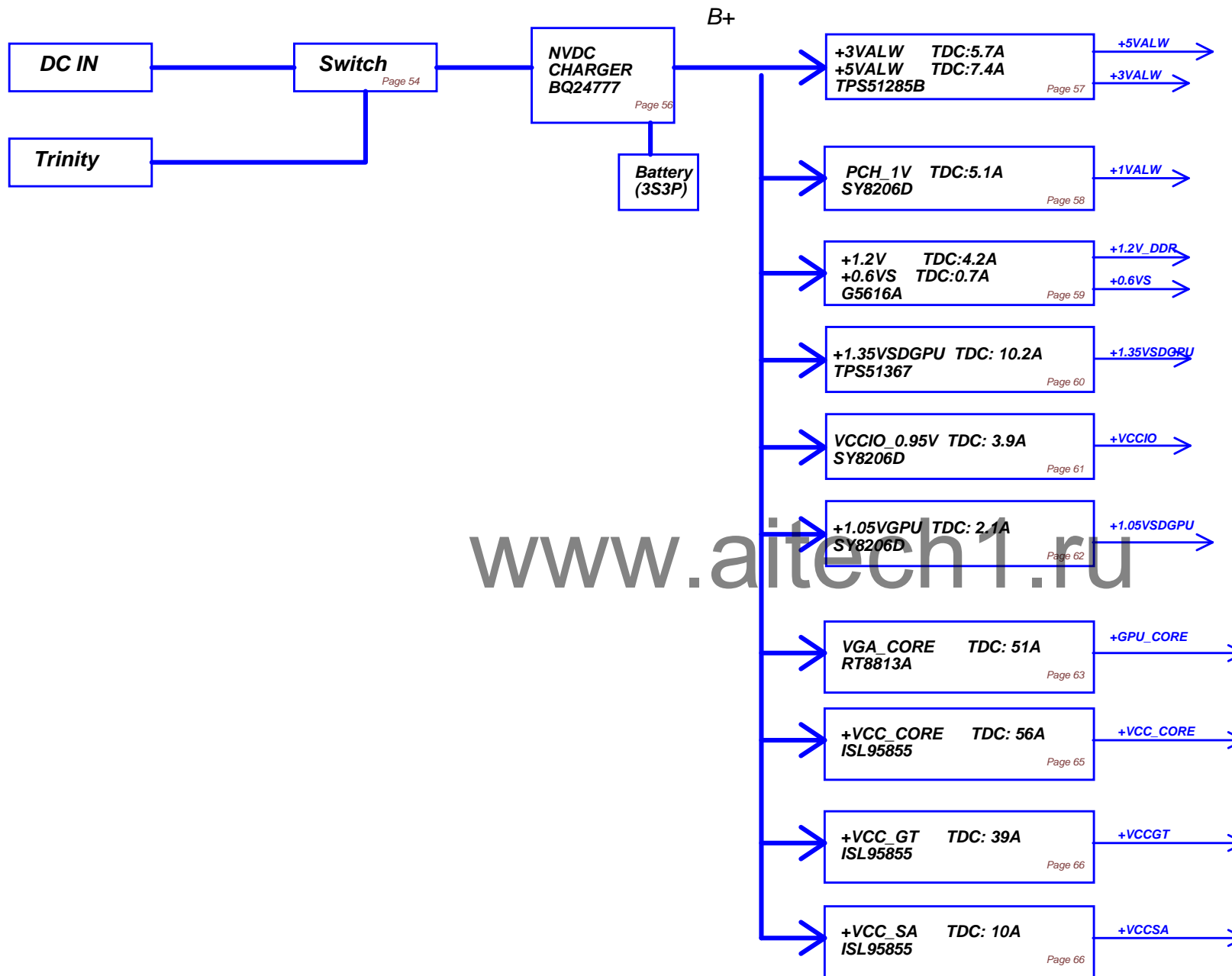
Screw Hole

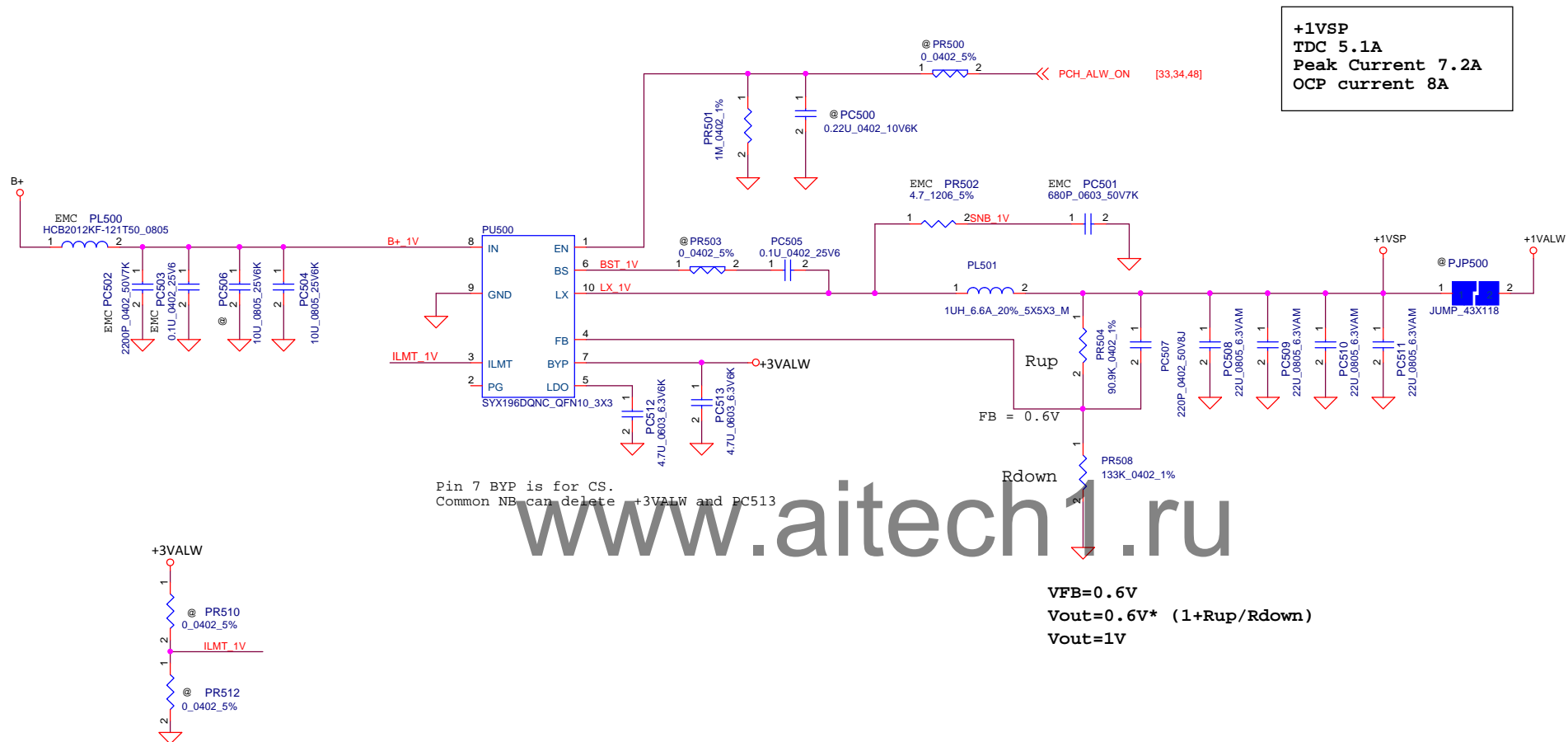


RTC Battery With Charge Function



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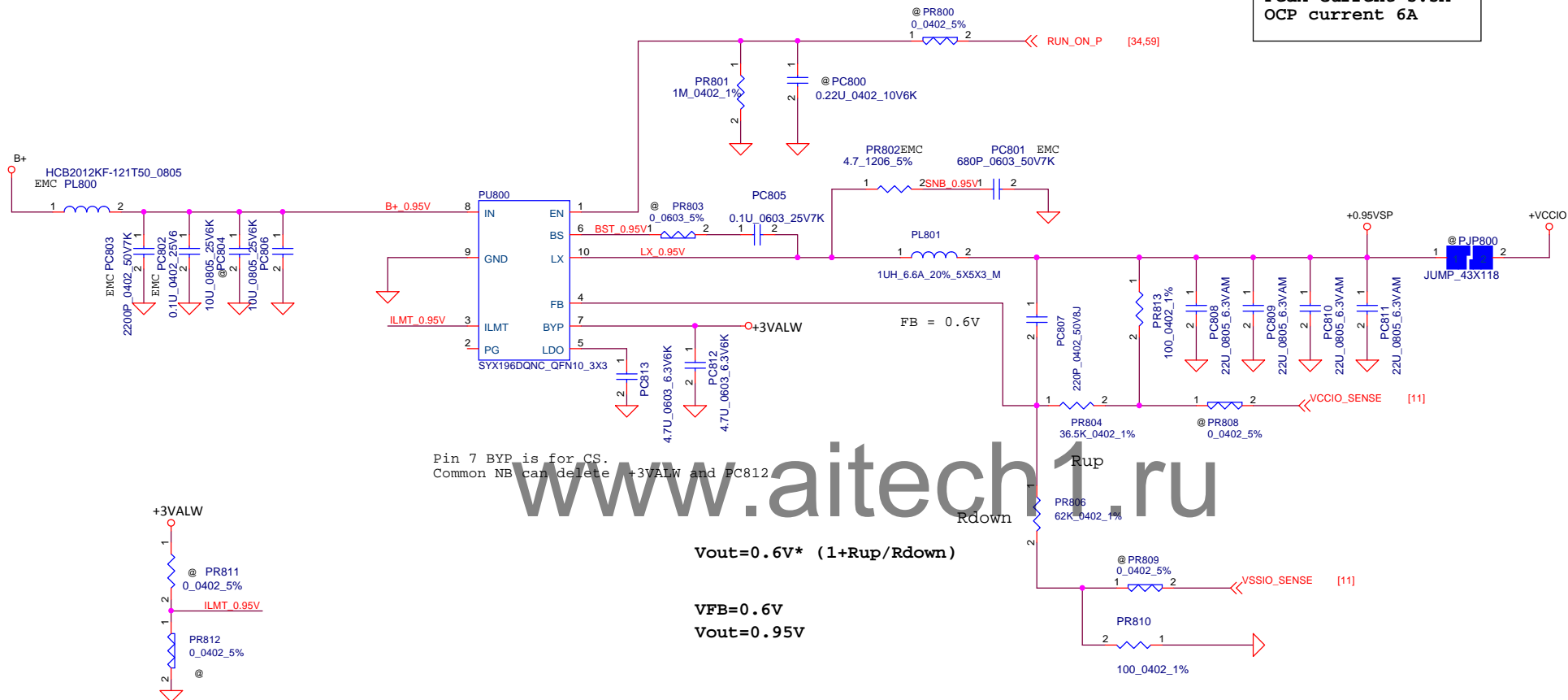


+1VSP
TDC 5.1A
Peak Current 7.2A
OCP current 8A

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

PWR.Plane.Regulator(35.25), Support component(35.26)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +IVA
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Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC812

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$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

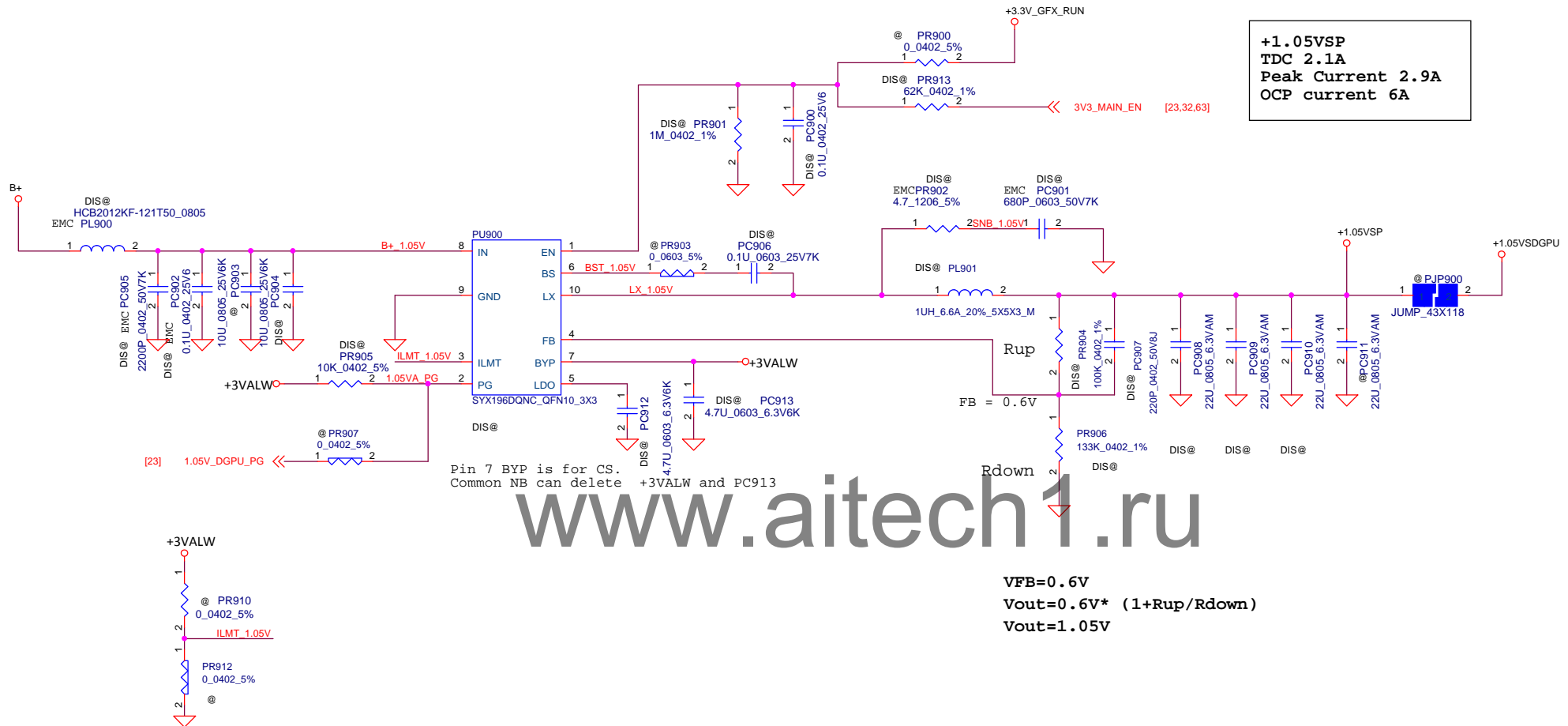
$$V_{FB} = 0.6V$$

$$V_{out} = 0.95V$$

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

1.05V controller(35.5), Support component(35.6)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +0.95VA
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+1.05VSP
TDC 2.1A
Peak Current 2.9A
OCP current 6A

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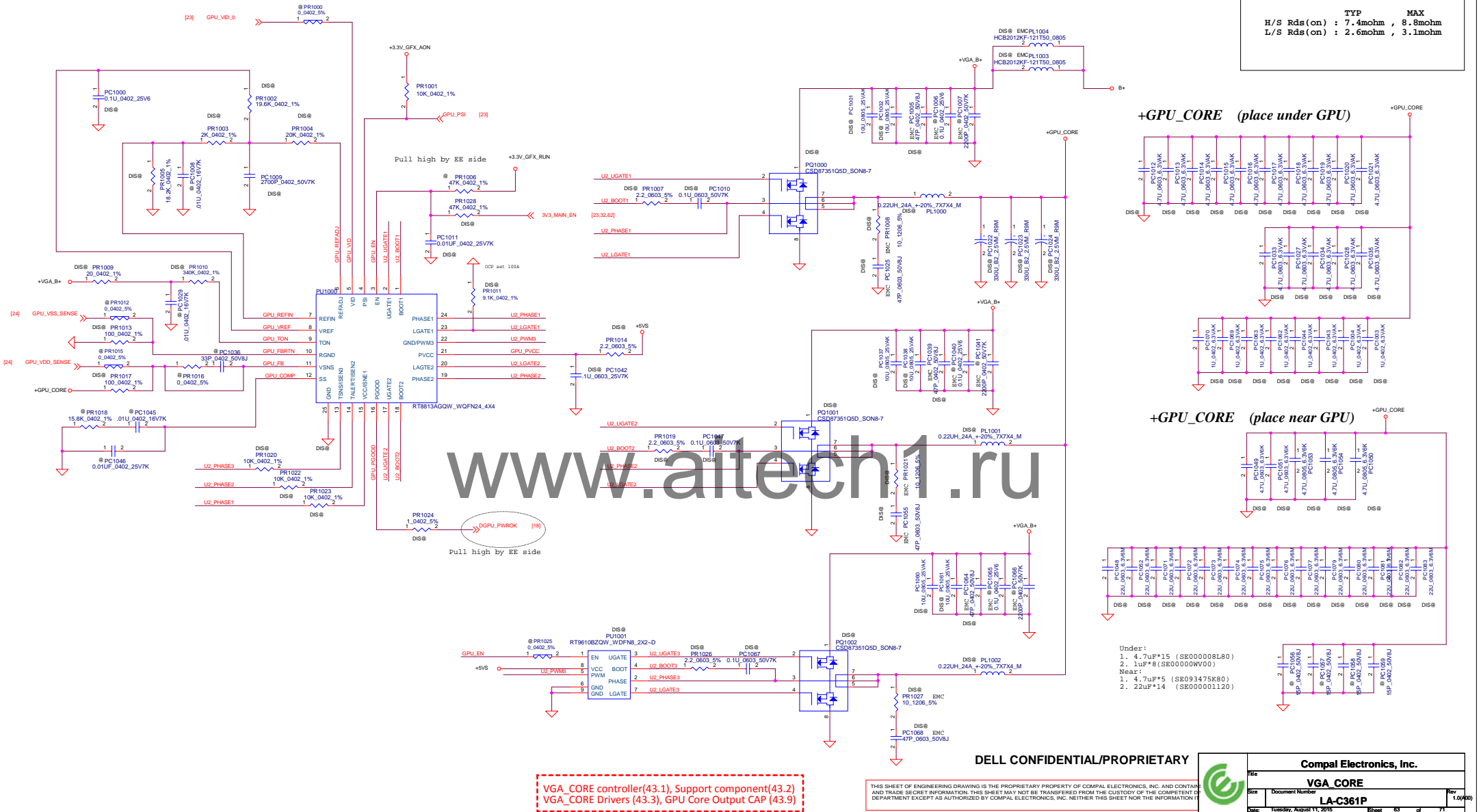
The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

GPU other power_Regulatorr(43.7), Support component(43.8)

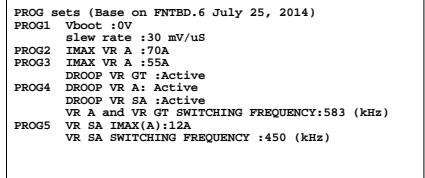
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +1.05VA	
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GPU_CORE (0.95V)
TDC 51A
Peak Current 87A
OCP current 100A
DCR 0.97mohm +/- 5%

TYP MAX
H/S Rds(on) : 7.4mohm , 8.8mohm
L/S Rds(on) : 2.6mohm , 3.1mohm

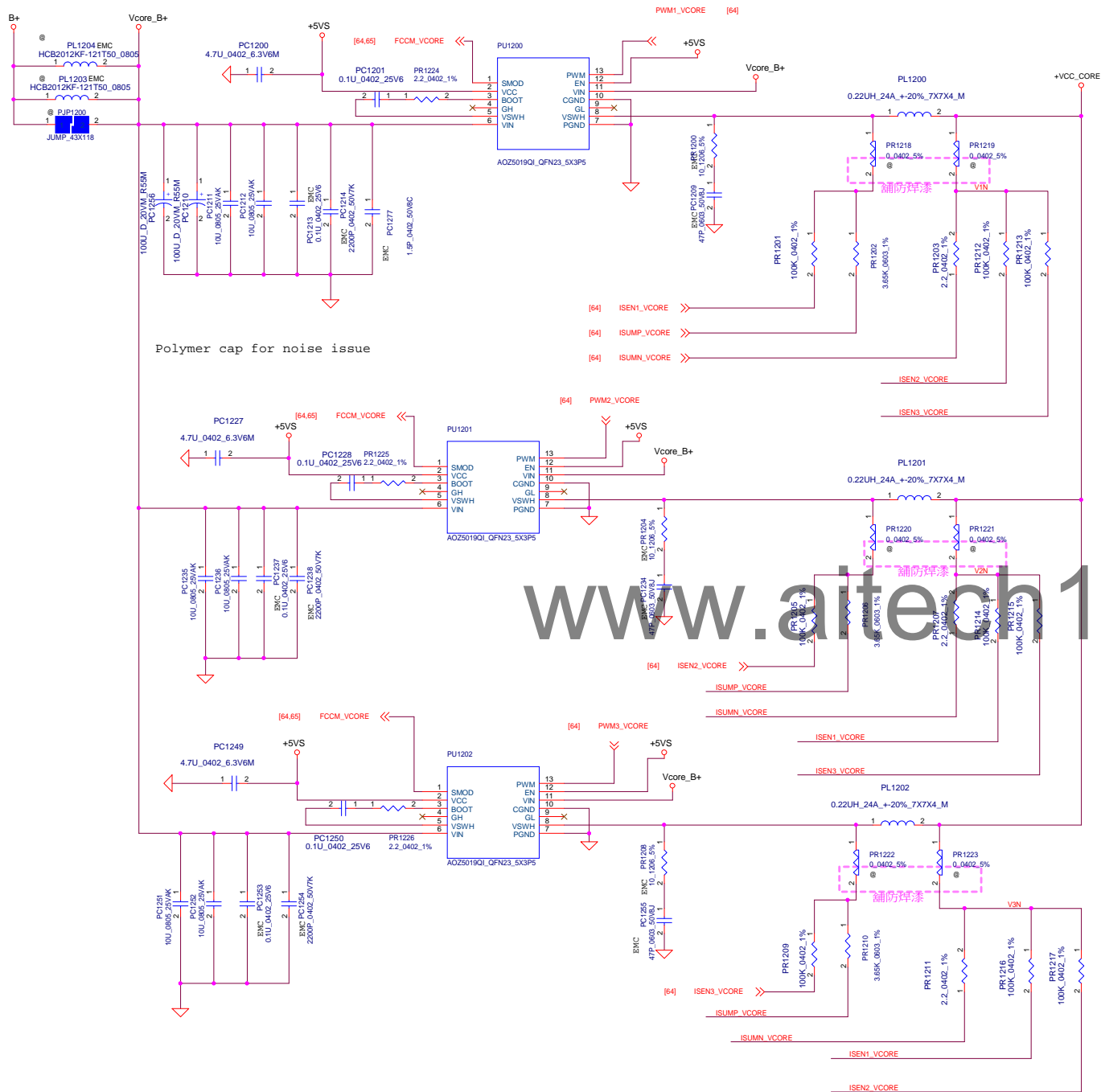


Compal Electronics, Inc.	
VGA CORE	
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CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)

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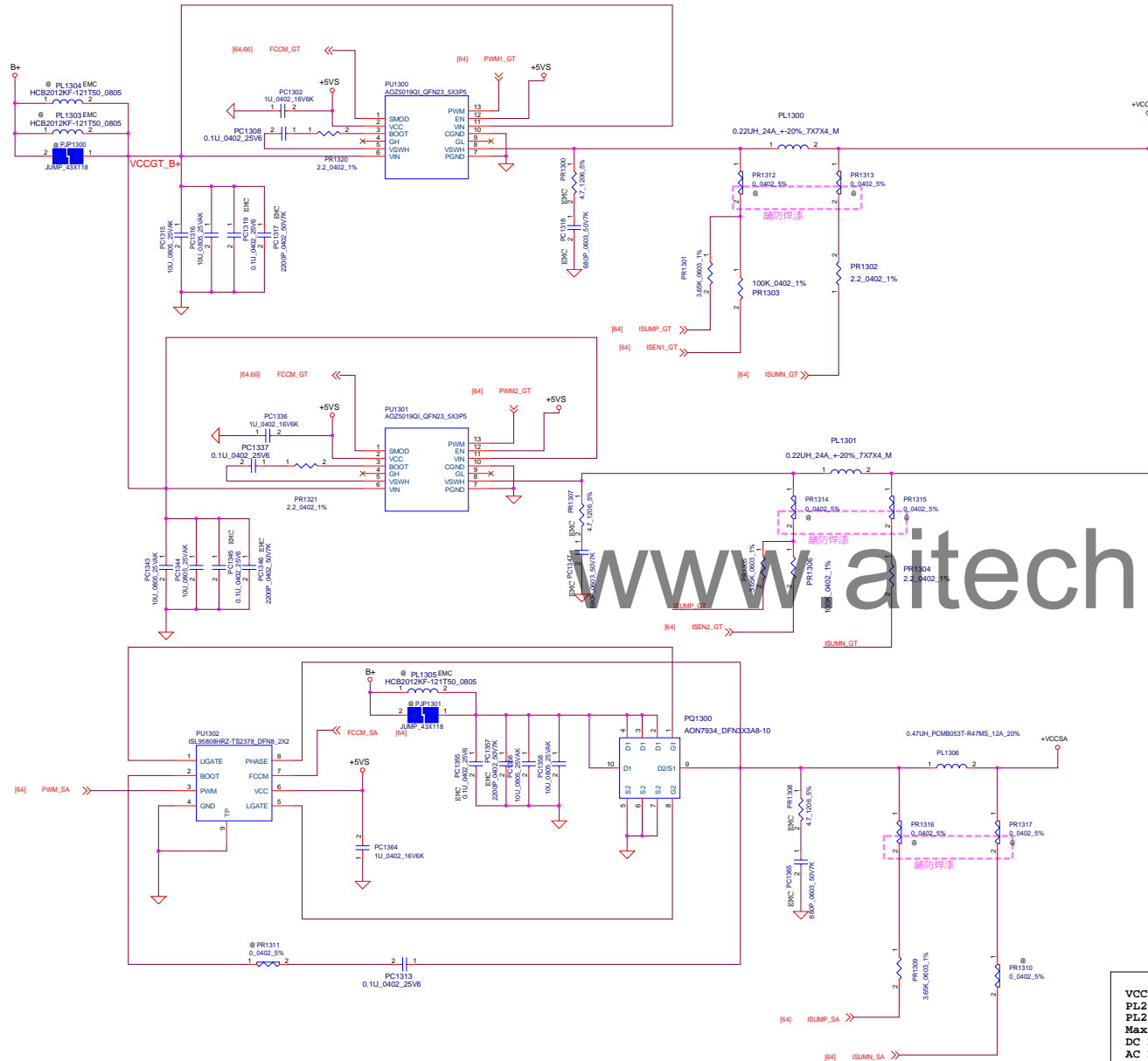
VCC_core (Base on PDDG rev 0.7)
 PL2 TDC_default):TB
 PL2 TDC_max (40Sec):56A
 Peak Current 68A
 DC Load line -1.8mV/A
 AC Load line -1.8mV/A
 OCP Current 83.2A
 DCR 0.97mohm +/-5%

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CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3),
 CPU_Core output CAP(36.4), Acoustic Noise B+ Bulk CAP(37.2)

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VCCGT (Base on PDDG rev 0.7)
 PL2 TDC_default):TB
 PL2 TDC_max (40Sec):39A
 Max Current 55A
 DC Load line -2.65mV/A
 AC Load line -2.65mV/A
 OCP Current 66.7A
 DCR 0.97mohm +/-5%



VCCSA (Base on PDDG rev 0.7)
 PL2 TDC_default):TBD
 PL2 TDC_max (40Sec):10A
 Max Current 11A
 DC Load line -9.1mV/A
 AC Load line -9.1mV/A
 OCP Current 20A
 DCR 7.4mohm/8.5mohm +/-5%

CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3),
 GFX output CAP(36.5)

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Description

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Description

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	XDP	2014/12/12	EE	Change Pull high power for leakage issue	Change RH494,RH495,RH496 from +VCCST to +VCCSTG, de-POP RH97,RH98,RH100, POP RH494,RH495.	X01
2	18	GPIO	2014/12/12	EE	Change Pull high power for double pull high the same power rail	Change RH571 power rail from +3VS to +3V_PCH, de-pop RH571, delete RH532.	X01
3	18	SPI	2014/12/12	EE	Change SPI ROM for ME register setting	Change UH8 from W25Q128FVSIQ_S08 to W25Q128FVSIQ_S08	X01
4	18	S0iX	2014/12/12	EE	Change by pass circuit design for CS mode function	Change RZ58 connection from UZ11.2 to UZ11.4, Change RZ60 connection from UZ12.2 to UZ12.4	X01
5	18	+1V_MPHY	2014/12/12	EE	Delete +1V_MPHY load switch & discharge circuit for useless.	Delete RH514,RH559,RH144,QH9,UH13,CH193,CH194,CH195. Delete net MPHPY_PWR_EN, move RZ70 to page 21	X01
6	18	PD	2014/12/22	EE	Update TI PD controller circuit follow Mirama	Update UTS from W25Q80BLZPIG_WSON8 to W25Q80DVSSIQ_S08,Delete RT166,Change net VCC3V3_TBTA_LDO to VCC3V3_FLASH. Change net VCC3V3_SX_SYS to +3VA_TBTA. Add RT198 to PWR_SRC_ILIMIT,Swap UT4.B2/C2 net. Update RT165 from 1206 to 0805, RT167,RT168, RT169,RT170,RT171,RT179,RT186,RT187,RT188,RT189,RT192,RT193,RT196,RT197 from 0402 to 0201. Add RT200,RT201 to net UPD_SMBDAT/UPD_SMBCLK"	X01
7	18	EC	2014/12/15	EE	Update Board ID for EC	Update RE67 to 62K	X01
8	18	PM	2014/12/15	EE	modify for support deep sleep function	De-pop RH506	X01
9	18	DDR	2014/12/15	EE	change Power rail for correct design	Change RH525 power rail from +3VALW to +3VS	X01
10	18	SPK	2014/12/15	EE	Add pull high resistor for MB side	Add RH572 to +3VS for SPK_DET#	X01
11	18	GPIO	2014/12/15	EE	Change GPIO for sync common GPIO table	Change net DGPU_PWR_EN from GPP_D13 to GPP_D12	X01
12	18	PD	2014/12/15	EE	Pin swap for DFB review	pin swap DT4,DT9	X01
13	18	PCH	2014/12/15	EE	Add Capacitor for follow Schematic check list	Add CH200 to +3V_PCH (Close to UH2.BA15)	X01
14	18	DIS	2014/12/15	EE	Add pull high resistor by vendor request	Add RPH34 replace to RV520,RV521,RV522 and add net THERMAL_ALERT#.	X01
15	18	SPI	2014/12/15	EE	Follow CRB XDP design	Add RH574,RH575 for SPI to XDP connector	X01
16	18	VDDQC	2014/12/16	EE	Follow CRB boardfile	POP RH473	X01
17	18	DEBUG	2014/12/16	EE	Add Debug signal by EC request	Change net BID_BC to GPP_C15, Add Net UARTT0_TX from GPP_C9 to JDEG1.pin 9	X01
18	18	DEBUG	2014/12/16	EE	Modify Debug UART from closed Chassis to Open Chassis	Delet UI6,RI29.Add JUART for UART2_TXD/UART2_RXD connect.	X01
19	18	SCI	2014/12/16	EE	Change PU resistor follow Miramar	RH383 change from 100K to 10K	X01
20	18	HOLE	2014/12/16	EE	Add 2 PAD for ME NUT	Add H50, H51	X01
21	18	EC	2014/12/16	EE	Add series resistor follow CRB	Add RE111 43K series S10_SLP_SUS#	X01
22	18	PCH	2014/12/16	EE	Change BOM to follow CRB	Change RH88 from 10K to 47K, De-POP RE33.	X01
23	18	EC	2014/12/17	EE	Modify GPIO for follow GPIO MAP by Dell	Add RE112 and Connect net BID_DIS to UE3.A10, swap Net BAT1_LED#(UE3.B1=>UE3.A40)/BAT2_LED#(UE3.A55=>UE3.B43)/PCH_PCIE_WAKE#(UE3.A40=>UE3.B46)/ME_FWP_EC(UE3.B46=>UE3.B1)/USB_PWR_SHR_LFT_EN#(UE3.B43=>UE3.A55)	X01
24	18	EC	2014/12/17	EE	Update BOM for design change	de-POP RE27, RE63, POP RH453	X01
25	18	NGFF	2014/12/17	EE	Update NGFF from Key E. to Key A.	Change JNGFF1 to CONCR_213AAAA32FA	
26	18	PCH	2014/12/17	EE	Change array resistor to resistor for routing	Change RP21 to RH576,RH577,RH578,RH579. Add RE113,RE114,RE115 for UE1.	
27	18	USB	2014/12/18	EE	Change net name by EC request	USB_PWR_SHR_VBUS_LFT_EN -> USB_PWR_SHR_VBUS_EN_L, USB_PWR_SHR_VBUS_RHT_EN1 -> USB_PWR_SHR_VBUS_EN_R, USB_PWR_SHR_LFT_EN# -> USB_PWR_SHR_EN_L#, USB_PWR_SHR_RHT_EN1# -> USB_PWR_SHR_EN_R#, USB2_DET_EC# -> USB_DET_EC_L#, USB1_DET_EC# -> USB_DET_EC_R#	
28	18	TS	2014/12/18	EE	Update Touch Screen Connector by ME request	Update JTS to ACES_50208-00601-P01	
29	18	USB	2014/12/18	EE	Add Pull down resistor for USB2.0	Add RH580,RH581 to UH2.AD10,UH2.AG2 to GND	
30	18	AR	2014/12/19	EE	Reserve test point for Alpine Ridge	Add T199,T200,T201	
31	18	PD	2014/12/22	EE	Delete common mode chok & ESD for vendor feedback	Delete LT10,DT5	
32	18	EC	2014/12/22	EE	Delete I2C signal from EC to Codec.	Delete QE14	
33							
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
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